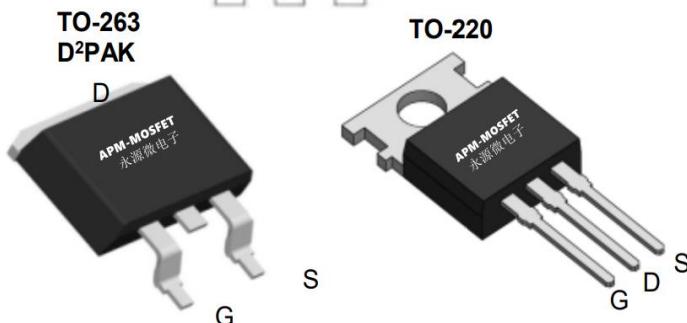
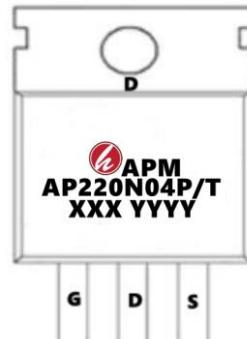
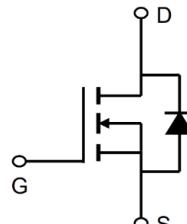


40V N-Channel Enhancement Mode MOSFET
Description

The AP220N04P/T uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.


General Features

$V_{DS} = 40V$ $I_D = 220A$

$R_{DS(ON)} < 2.5m\Omega$ @ $V_{GS}=10V$ (Type: **1.9mΩ**)

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP220N04P	TO-220-3L	AP220N04P XXX YYYY	1000
AP220N04T	TO-263-3L	AP220N04P XXX YYYY	800

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

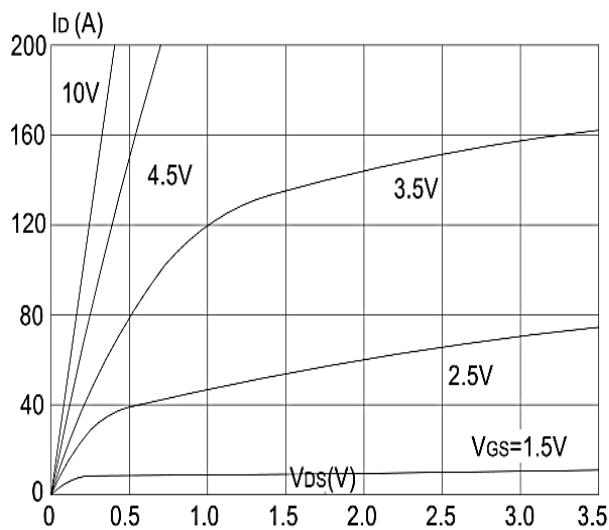
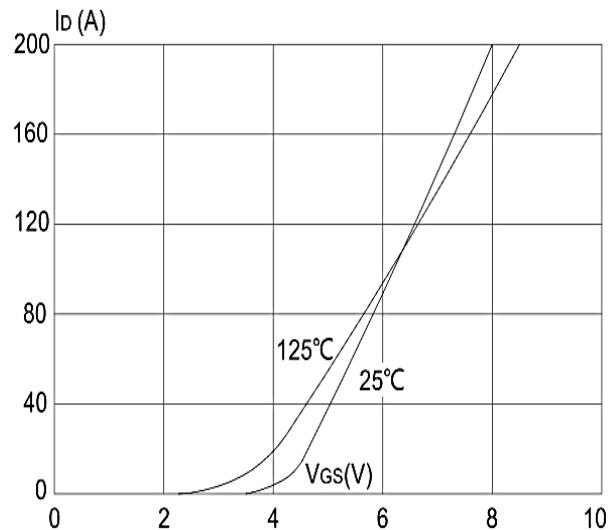
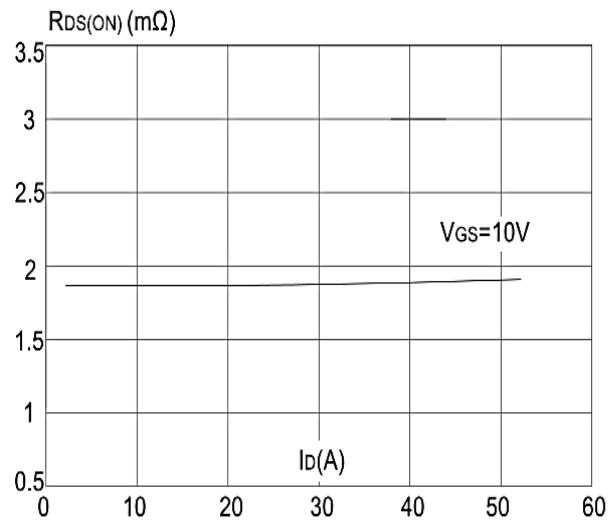
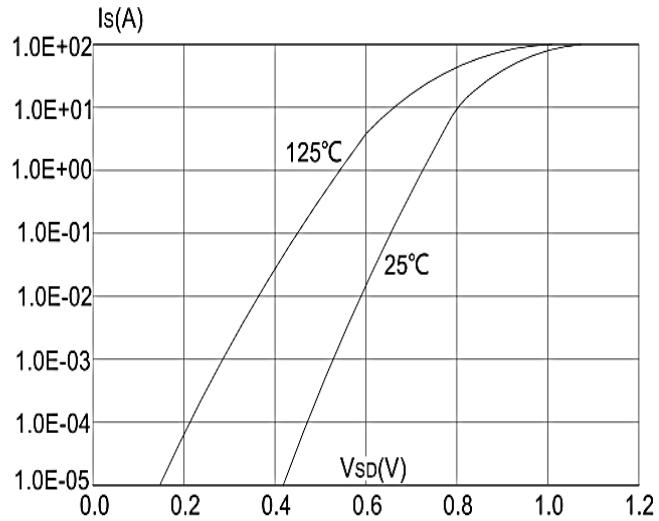
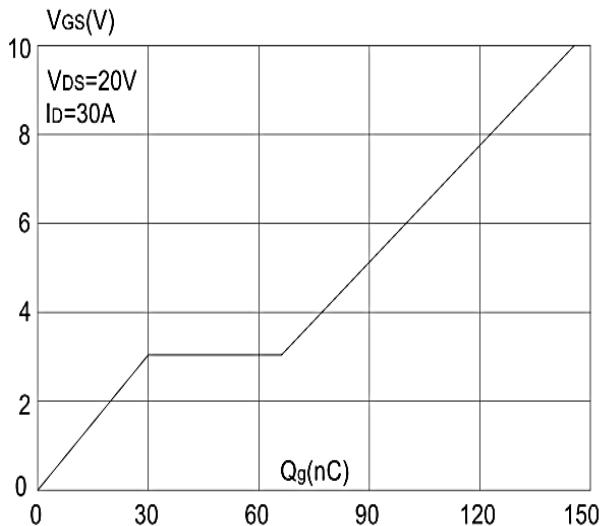
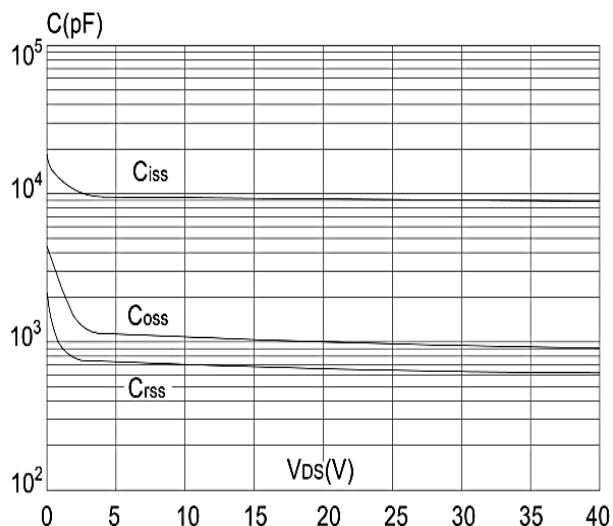
Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	220	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	124	A
I_{DM}	Pulsed Drain Current ²	760	A
E_{AS}	Single Pulse Avalanche Energy ³	576	mJ
I_{AS}	Avalanche Current	48	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation ⁴	197	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) ¹	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	0.76	°C/W

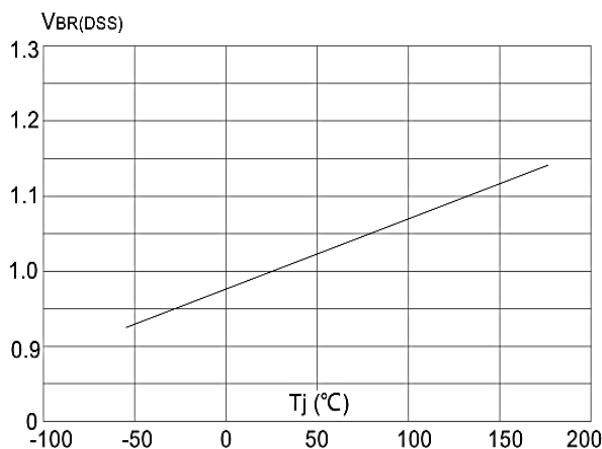
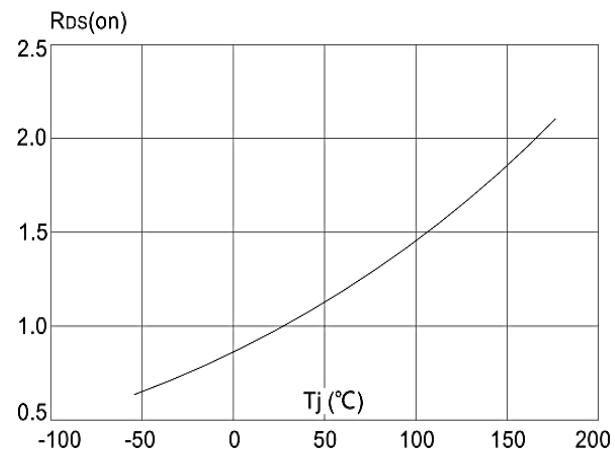
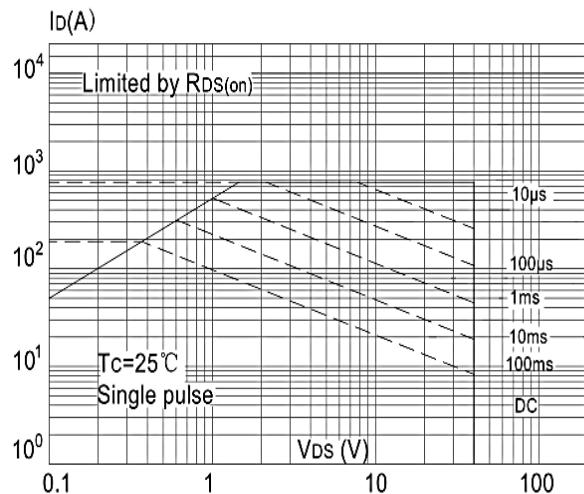
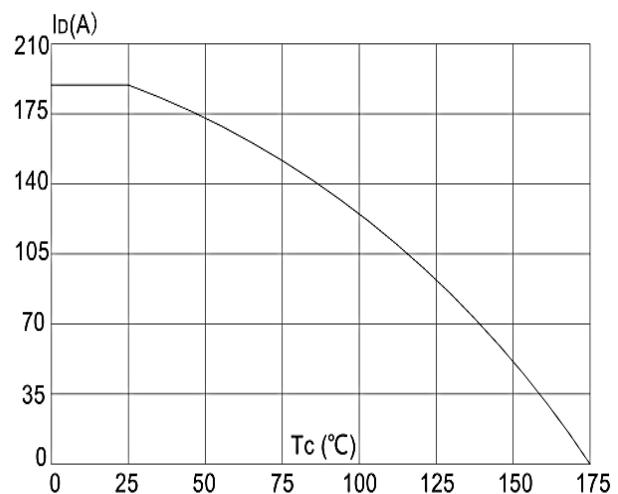
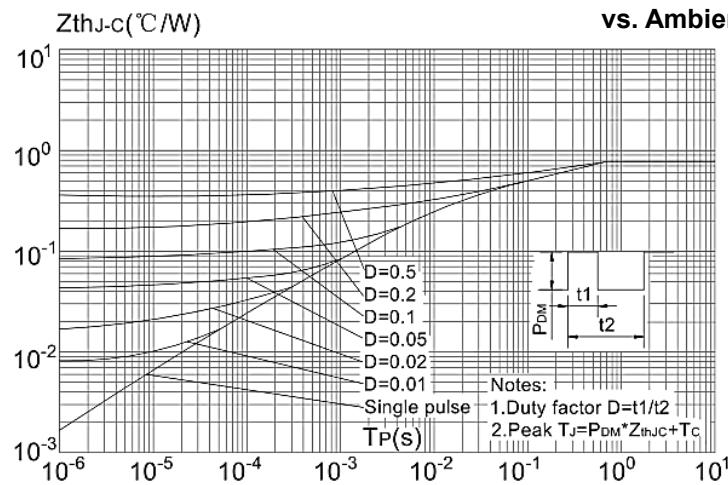
40V N-Channel Enhancement Mode MOSFET
Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	49	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±25V	-	-	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2	2.8	4	V
R _{DS(on)}	Static Drain-Source on-Resistance	V _{GS} =10V, I _D =30A	-	1.9	2.5	mΩ
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1.0MHz	-	9060	-	pF
C _{oss}	Output Capacitance		-	1000	-	pF
C _{rss}	Reverse Transfer Capacitance		-	666	-	pF
Q _g	Total Gate Charge	V _{DS} =20V, I _D =30A, V _{GS} =10V	-	145	-	nC
Q _{gs}	Gate-Source Charge		-	30	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	37	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =30A, R _L =1Ω, R _{GEN} =3Ω, V _{GS} =10V	-	39	-	ns
t _r	Turn-on Rise Time		-	56	-	ns
t _{d(off)}	Turn-off Delay Time		-	108	-	ns
t _f	Turn-off Fall Time		-	71	-	ns
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	220	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	760	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =30A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	T _J =25°C, I _F =20A, dI/dt=100A/μs	-	50	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	81	-	nC

Note :

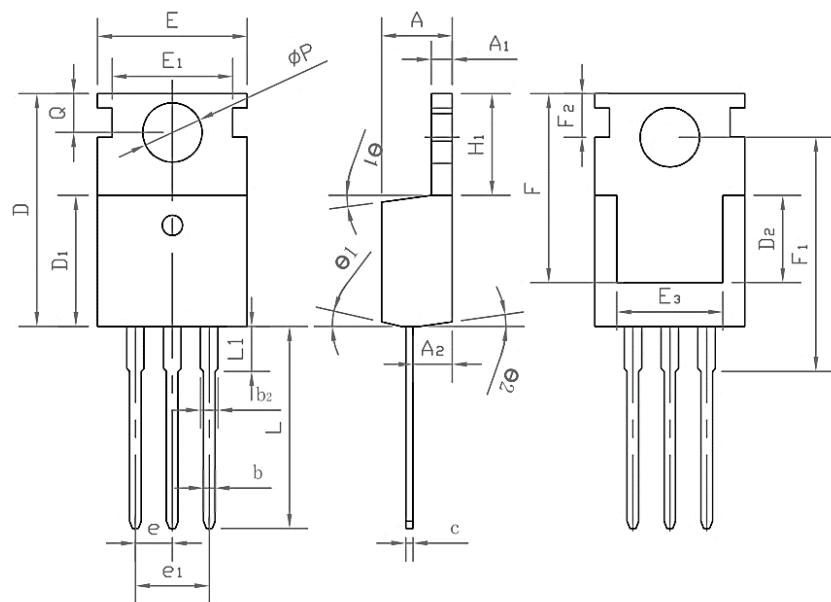
1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%
3. The EAS data shows Max. rating . The test condition is T_J=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25Ω, I_{AS}=48A
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

40V N-Channel Enhancement Mode MOSFET
Typical Characteristics

Figure 1: Output Characteristics

Figure 2: Typical Transfer Characteristics

Figure 3: On-resistance vs. Drain Current

Figure 4: Body Diode Characteristics

Figure 5: Gate Charge Characteristics

Figure 6: Capacitance Characteristics

40V N-Channel Enhancement Mode MOSFET

Figure 7: Normalized Breakdown Voltage vs Junction Temperature

Figure 8: Normalized on Resistance vs. Junction Temperature

Figure 9: Maximum Safe Operating Area

Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

40V N-Channel Enhancement Mode MOSFET

Package Mechanical Data-TO-220-3L-SLK



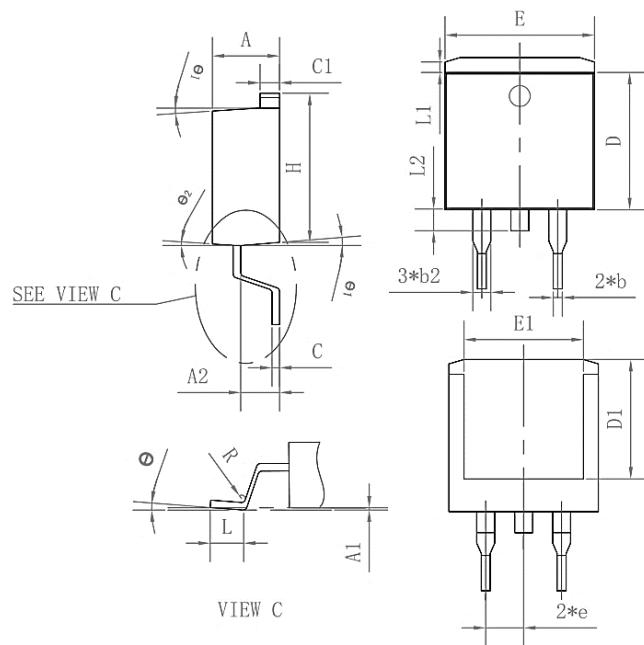
Symbol	Common		
	Mim	mm	Max
A	4.27	4.57	4.87
A1	1.15	1.30	1.45
A2	2.10	2.40	2.70
b	0.70	0.80	1.00
b2	1.17	1.27	1.50
D	0.40	0.50	0.65
D1	8.80	9.10	9.40
D2	5.70	6.70	7.00
E	9.70	10.00	10.30
E1	-	8.70	-
E2	9.63	10.00	10.35
E3	7.00	8.00	8.40
e		0.37	
e1		0.10	
H1	6.00	6.50	6.85
L	12.75	13.50	13.90
L1	-	3.10	3.40
Φp	3.45	3.60	3.75
Q	2.60	2.80	3.00
θ1	4°	7°	10°
θ2	0°	3°	6°
F	13.30	13.50	13.70
F1	15.50	15.90	16.30
F2	2.80	3.00	3.20

**APM**

A Power Microelectronics

AP220N04P/T

40V N-Channel Enhancement Mode MOSFET
Package Mechanical Data-TO-263-3L-SLK



Symbol	Common mm		
	Mim	Nom	Max
A	4.35	4.47	4.60
A1	0.09	0.10	0.11
A2	2.30	2.40	2.70
b	0.70	0.80	1.00
b2	1.25	1.36	1.50
C	0.45	0.50	0.65
C1	1.29	1.30	9.40
D	9.10	9.20	9.30
D1	7.90	8.00	8.10
E	9.85	10.00	10.20
E1	7.90	8.00	8.10
H	15.30	15.50	15.70
e	-	2.54	-
L	2.34	2.54	2.74
L1	1.00	1.10	1.20
L2	1.30	1.40	1.50
R	0.24	0.25	0.26
θ	0°	4°	8°
θ1	4°	7°	10°
θ2	0°	3°	6°

40V N-Channel Enhancement Mode MOSFET**Attention**

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40V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2023/8/1	Initial release

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