HARRIS SEMICONDUCTOR

HGTG12N60C3DR, HGTP12N60C3DR, HGT1S12N60C3DR, HGT1S12N60C3DRS

24A, 600V, Rugged, UFS Series N-Channel IGBT with Anti-Parallel Ultrafast Diode

February 1998

Features

- 24A, 600V at $T_C = 25^oC$
- 600V Switching SOA Capability
- Typical Fall Time at $T_J = 150^oC$ 250ns
- Short Circuit Rating at $T_J = 150^oC$ 10μs
- Low Conduction Loss
- Ultrafast Anti-Parallel Diode
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
HGTP12N60C3DR	TO-220AB	12N60CDR
HGT1S12N60C3DR	TO-262AA	12N60CDR
HGT1S12N60C3DRS	TO-263AB	12N60CDR
HGTG12N60C3DR	TO-247	12N60C3DR

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, ie., HGT1S12N60C3DRS9A.

Description

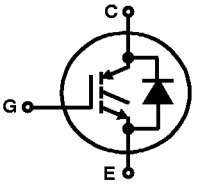
This family of IGBTs was designed for optimum performance in the demanding world of motor control operation as well as other high voltage switching applications. These devices demonstrate RUGGED performance capability when subjected to harsh SHORT CIRCUIT WITHSTAND TIME (SCWT) conditions. The parts have ULTRAFAST (UFS) switching speed while the on-state conduction losses have been kept at a low level.

The electrical specifications include typical Turn-On and Turn-Off dv/dt ratings. These ratings and the Turn-On ratings include the effect of the diode in the test circuit (Figure 17). The data was obtained with the diode at the same T_J as the IGBT under test. The diode used in anti-parallel with the IGBT is development type TA49213. The IGBT is development type TA49118.

Formerly development type TA49124.

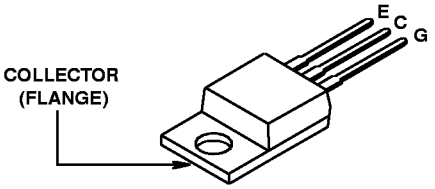
Terminal Diagram

N-CHANNEL ENHANCEMENT MODE

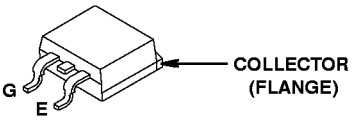


Packaging

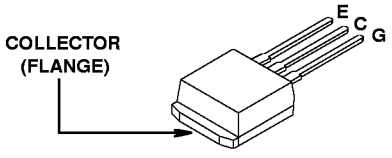
JEDEC TO-220AB (ALTERNATE VERSION)



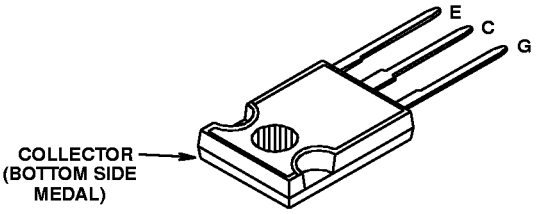
JEDEC TO-263AB



JEDEC TO-262AA



JEDEC TO-247AB



HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4467**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

			UNITS
Collector to Emitter Voltage	BV_{CES}	600	V
Collector Current Continuous			
At $T_C = 25^oC$	I_{C25}	24	A
At $T_C = 110^oC$	I_{C110}	12	A
Collector Current Pulsed (Note 1)	I_{CM}	48	A
Gate to Emitter Voltage Continuous	V_{GES}	±20	V
Gate to Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_C = 150^oC$	SSOA	48A at 600V	
Power Dissipation Total at $T_C = 25^oC$	P_D	104	W
Power Dissipation Derating $T_C > 25^oC$		0.83	$W/^oC$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Tech Brief 334	T_{pkg}	260	^oC
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	10	µs

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 440V$, $T_J = 150^oC$, $R_{GE} = 25\Omega$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	600	-	-	V
Collector to Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	-	-	250	µA
		$V_{CE} = BV_{CES}$, $T_C = 150^oC$	-	-	1.0	mA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	-	1.9	2.2	V
		$I_C = I_{C110}$, $V_{GE} = 15V$, $T_C = 150^oC$	-	2.0	2.5	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	4.5	6.1	7.5	V
Gate to Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$	-	-	±100	nA
Switching SOA (See Figure 2)	SSOA	$T_J = 150^oC$, $R_G = 25\Omega$, $V_{GE} = 15V$ $V_{CE(PK)} = 600V$, $L = 100\mu H$	48	-	-	A
Gate to Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	-	9.7	-	V
On-State Gate Charge	$Q_{g(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{ES}$, $V_{GE} = 15V$	-	50	70	nC
		$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{ES}$, $V_{GE} = 20V$	-	71	90	nC
Current Turn-On Delay Time	$t_{d(ON)I}$	$T_J = 25^oC$ $I_{CE} = I_{C110}$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 25\Omega$ $L = 1mH$ Diode used in test circuit RURP1560 at 25^oC	-	37	-	ns
Current Rise Time	t_{rI}		-	37	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	120	260	ns
Current Fall Time	t_{fI}		-	110	160	ns
Turn-On Energy (Note 4)	E_{ON}		-	400	450	µJ
Turn-Off Energy (Note 5)	E_{OFF}			340	700	µJ

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Turn-On Delay Time	$t_{d(ON)I}$	$T_J = 150^oC$ $I_{CE} = I_{C110}$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 25\Omega$ L = 1mH Diode used in test circuit RURP1560 at 150^oC	-	36	-	ns
Current Rise Time	t_{rI}		-	38	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$		-	290	500	ns
Current Fall Time	t_{fI}		-	250	400	ns
Turn-Off Voltage dv/dt (Note 3)	dV_{CE}/dt		-	2	-	V/ns
Turn-On Voltage dv/dt (Note 3)	dV_{CE}/dt		-	10	-	V/ns
Turn-On Energy (Note 4)	E_{ON}		-	0.83	0.91	mJ
Turn-Off Energy (Note 5)	E_{OFF}		-	1.20	1.95	mJ
Diode Forward Voltage	V_{EC}	$I_{EC} = 12A$	-	1.3	1.6	V
Diode Reverse Recovery Time	t_{rr}	$I_{EC} = 1A$, $dI_{EC}/dt = 200A/\mu s$	-	-	35	ns
		$I_{EC} = 12A$, $dI_{EC}/dt = 200A/\mu s$	-	-	60	ns
Thermal Resistance Junction to Case	$R_{\theta JC}$	IGBT	-	-	1.2	$^oC/W$
		Diode	-	-	1.75	$^oC/W$

NOTES:

3. dV_{CE}/dt depends on the diode used and the temperature of the diode.
4. Turn-On Energy Loss (E_{ON}) includes losses due to the diode recovery and is defined as the integral of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the collector voltage equals $V_{CE}(ON)$. This value of E_{ON} was obtained with a RURP1560 diode at $T_J = 150^oC$. A different diode or temperature will result in a different E_{ON}. For example with diode at $T_J = 25^oC$, E_{ON} is about one half the value of E_{ON} with diode at $T_J = 150^oC$.
5. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). All devices were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

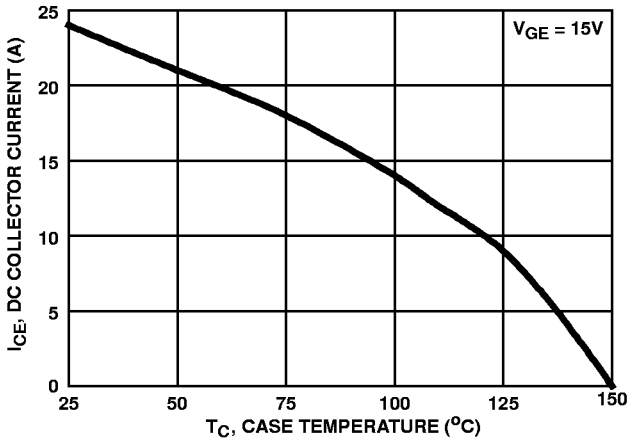


FIGURE 1. DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

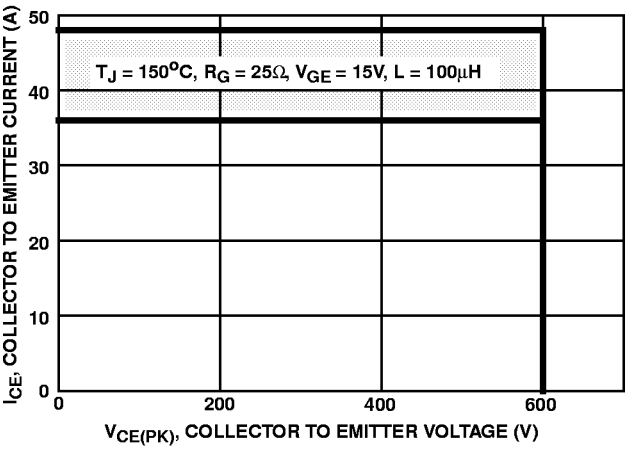


FIGURE 2. SWITCHING SAFE OPERATING AREAS

Typical Performance Curves (Continued)

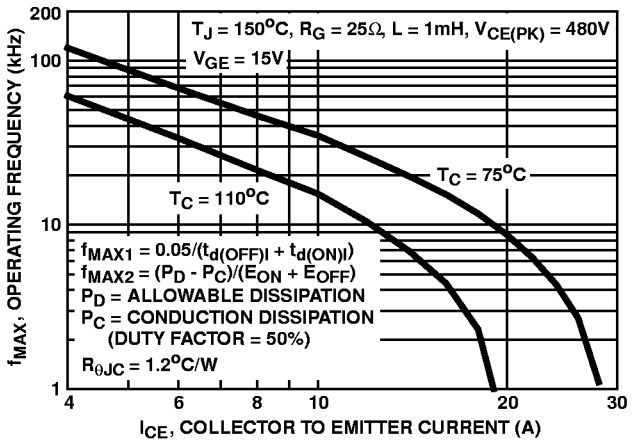


FIGURE 3. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

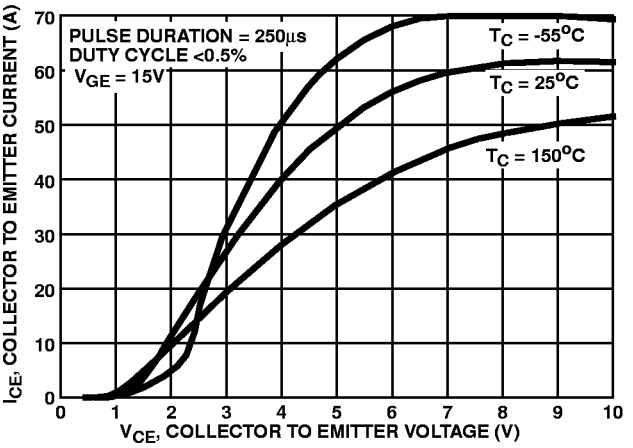


FIGURE 4. COLLECTOR TO EMITTER ON STATE VOLTAGE

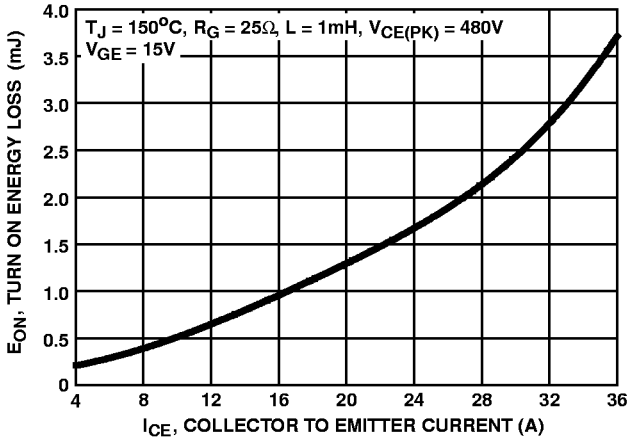


FIGURE 5. TURN ON ENERGY LOSS AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

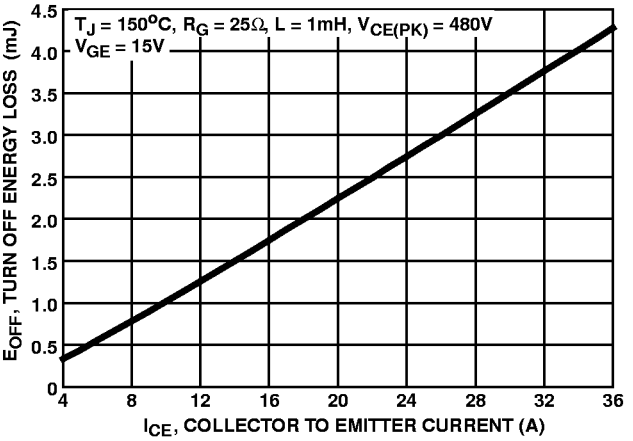


FIGURE 6. TURN OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

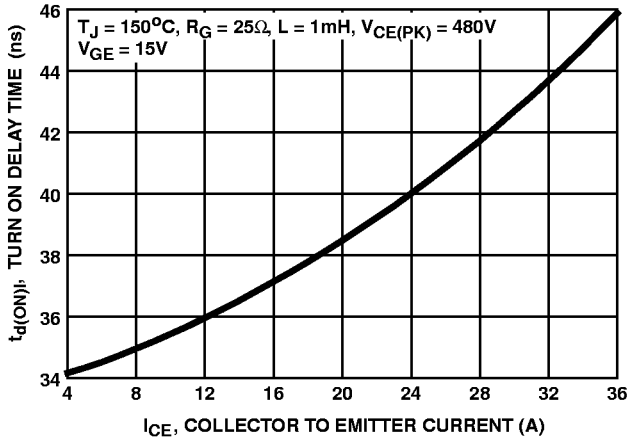


FIGURE 7. TURN ON DELAY TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

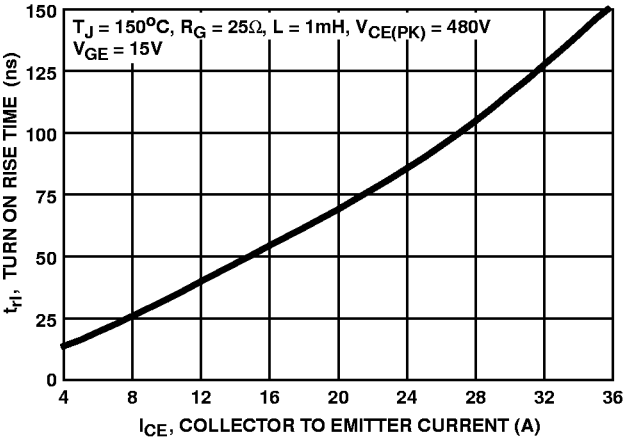


FIGURE 8. TURN ON RISE TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

Typical Performance Curves (Continued)

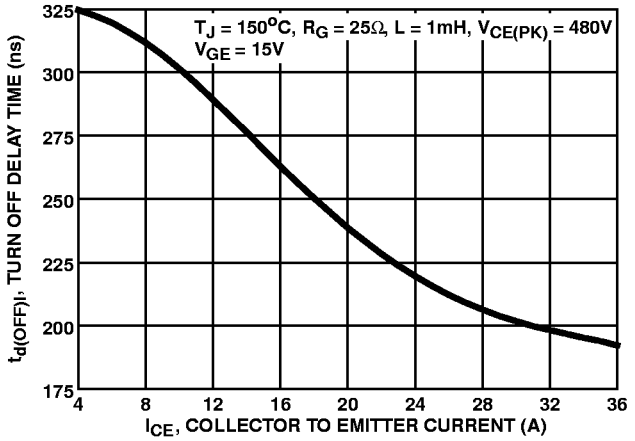


FIGURE 9. TURN OFF DELAY TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

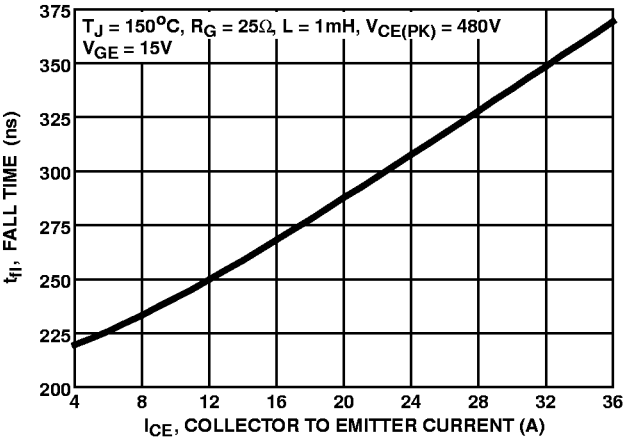


FIGURE 10. TURN OFF FALL TIME AS A FUNCTION OF COLLECTOR TO EMITTER CURRENT

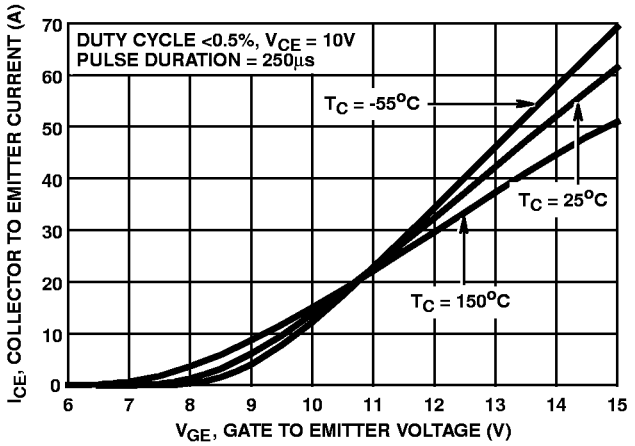


FIGURE 11. TRANSFER CHARACTERISTICS

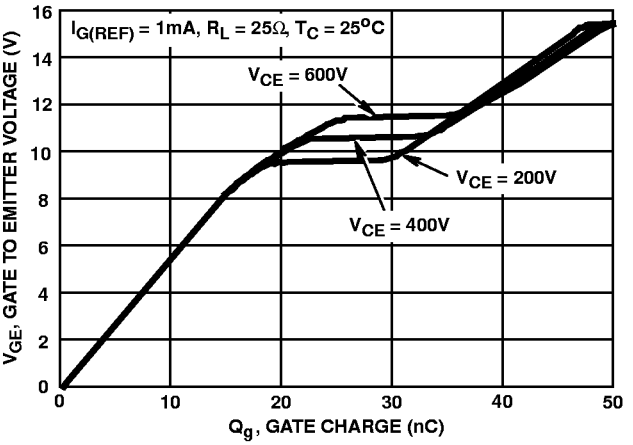


FIGURE 12. GATE CHARGE WAVEFORMS

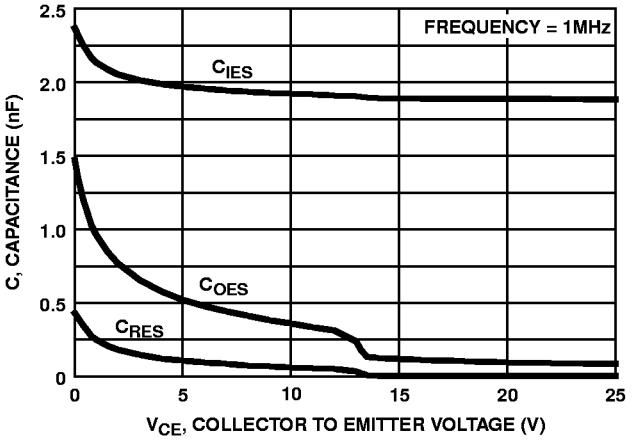


FIGURE 13. CAPACITANCE AS A FUNCTION OF COLLECTOR TO EMITTER VOLTAGE

Typical Performance Curves (Continued)

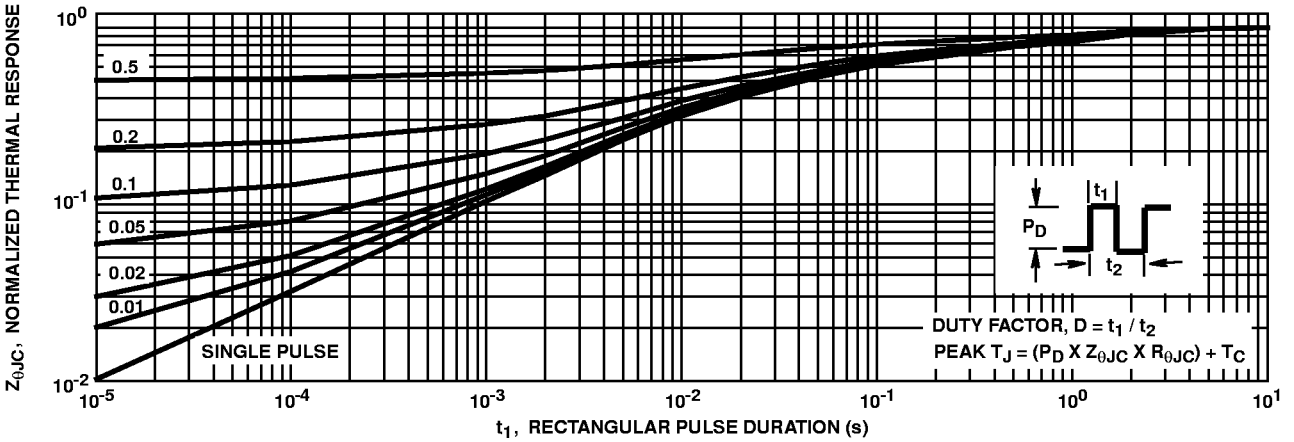


FIGURE 14. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

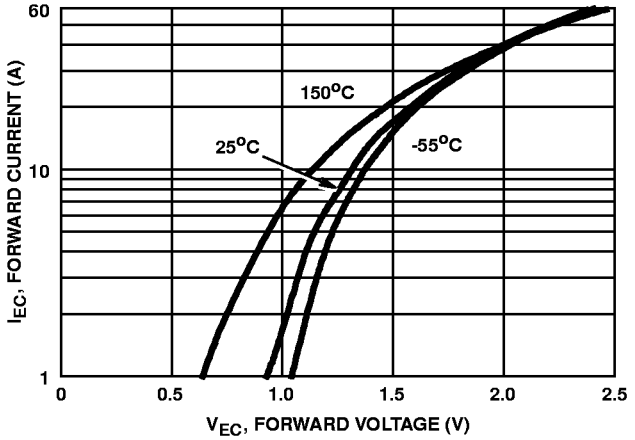


FIGURE 15. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

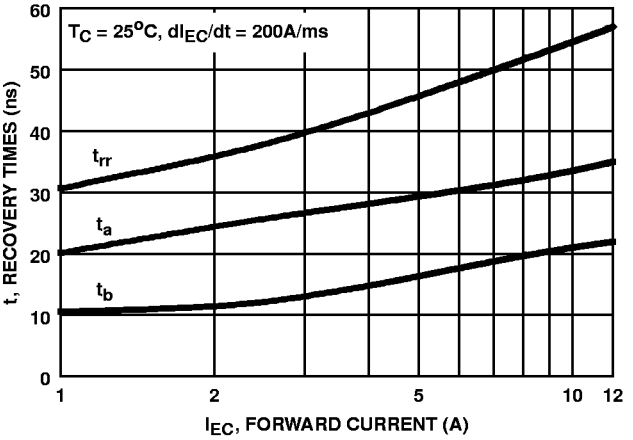


FIGURE 16. RECOVERY TIME AS A FUNCTION OF FORWARD CURRENT

Test Circuit and Waveforms

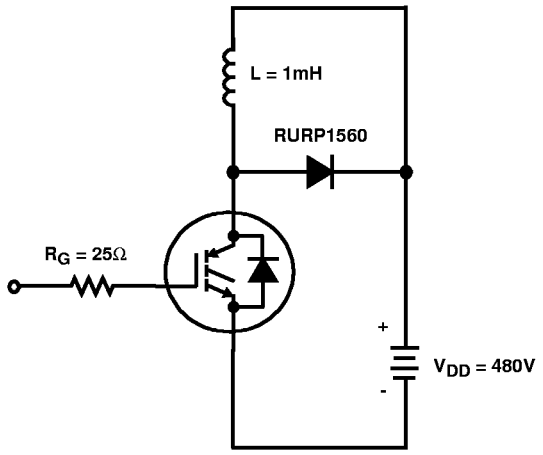


FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUIT

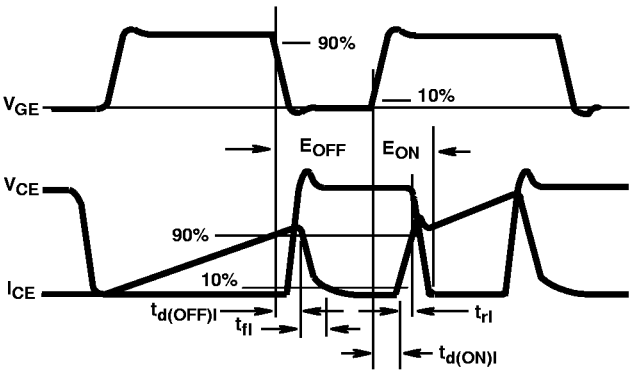


FIGURE 18. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 5, 6, 7 and 9. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 18. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(OFF)}$ is important when controlling output ripple under a lightly loaded condition.

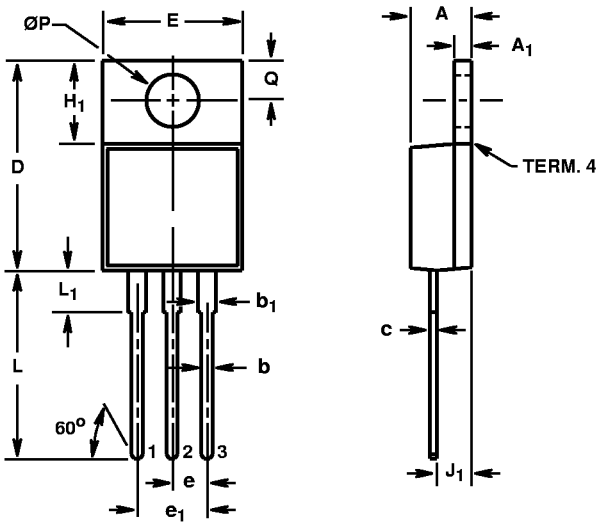
f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$.The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 18. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

ECCOSORBD™ is a trademark Emerson and Cumming, Inc.

TO-220AB (Alternate Version)

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



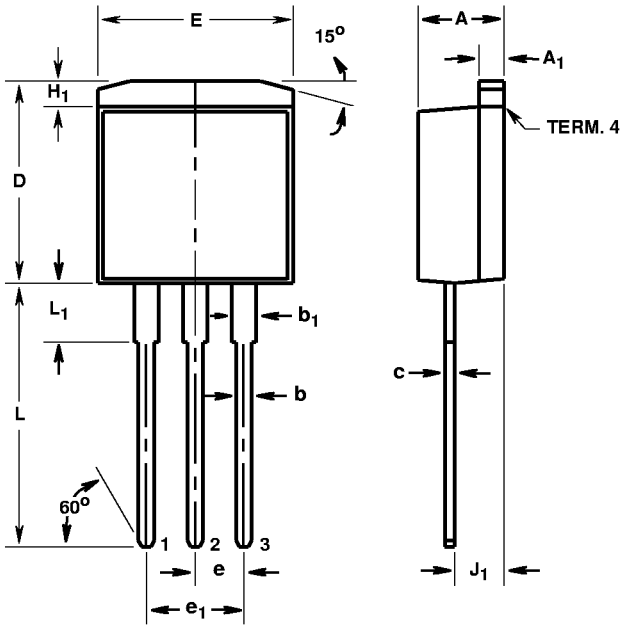
LEAD NO. 1 - GATE
LEAD NO. 2 - COLLECTOR
LEAD NO. 3 - EMITTER
TERM. 4 - COLLECTOR

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	2, 4
b	0.030	0.034	0.77	0.86	2, 4
b_1	0.045	0.055	1.15	1.39	2, 4
c	0.018	0.022	0.46	0.55	2, 4
D	0.590	0.610	14.99	15.49	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	3
ØP	0.149	0.153	3.79	3.88	-
Q	0.105	0.115	2.66	2.92	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Dimension (without solder).
3. Solder finish uncontrolled in this area.
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 3 dated 7-97.

TO-262AA 3 LEAD JEDEC TO-262AA PLASTIC PACKAGE

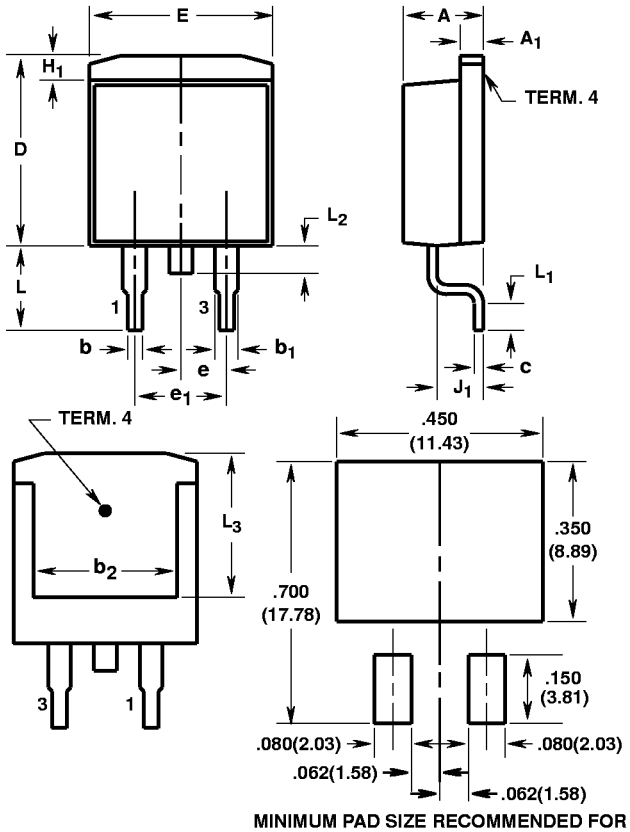


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 5 dated 7-97.

TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

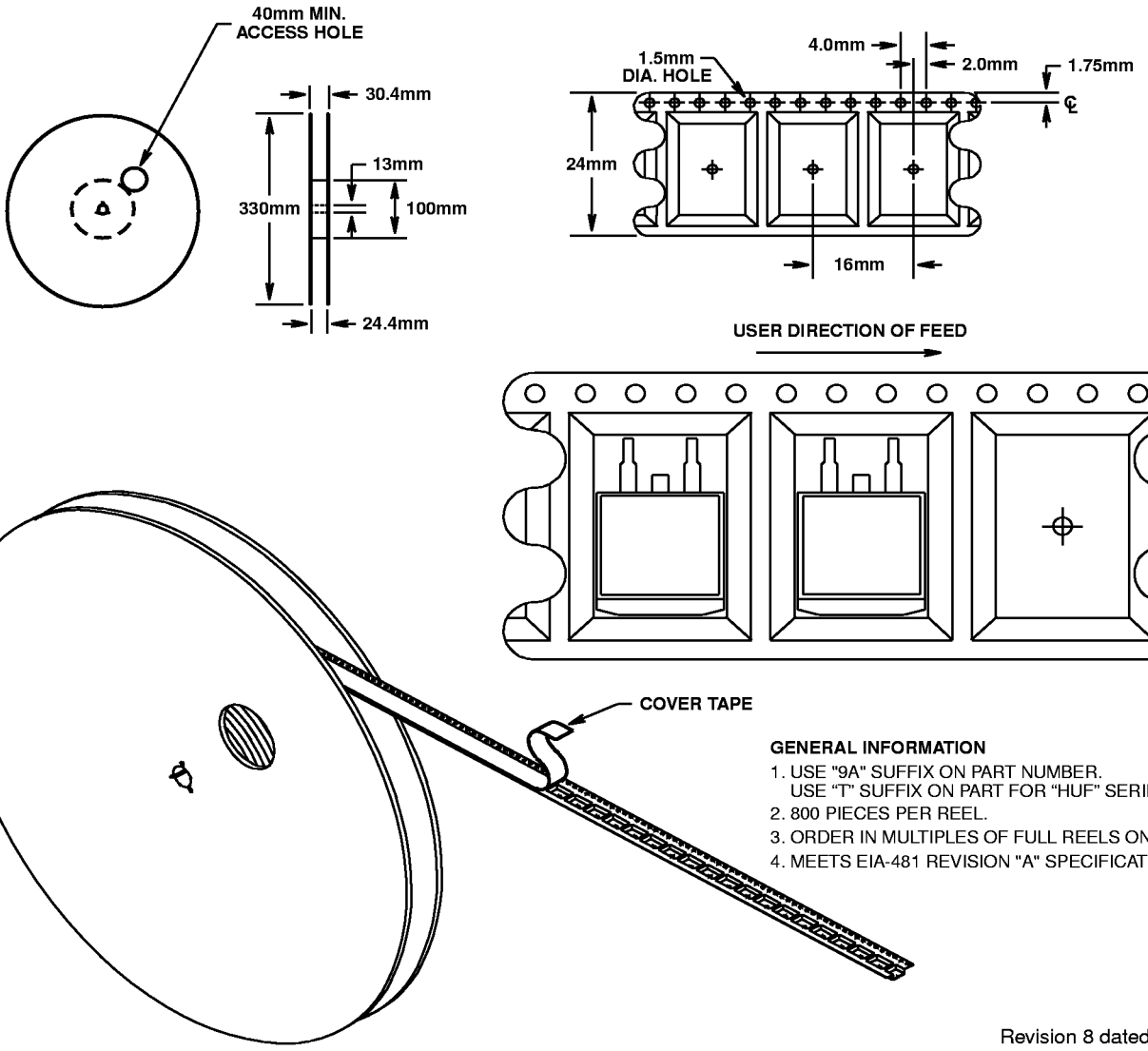
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:

9. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
10. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
11. Solder finish uncontrolled in this area.
12. Dimension (without solder).
13. Add typically 0.002 inches (0.05mm) for solder plating.
14. L_1 is the terminal length for soldering.
15. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
16. Controlling dimension: Inch.
17. Revision 8 dated 7-97.

TO-263AB

24mm TAPE AND REEL



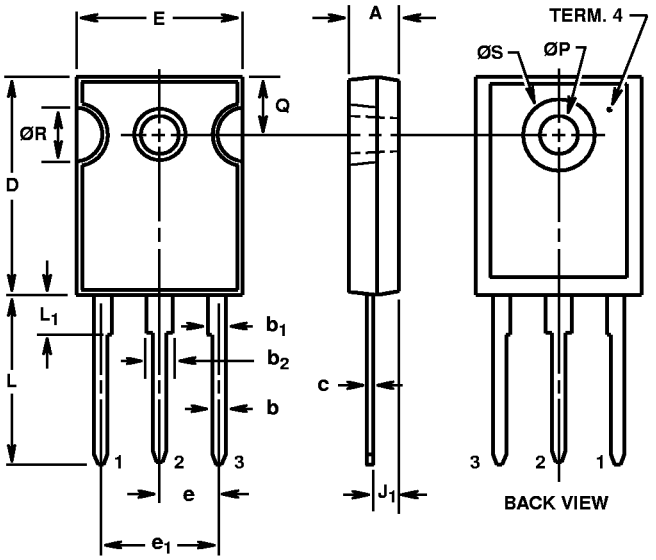
GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
   USE "T" SUFFIX ON PART FOR "HUF" SERIES.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 8 dated 7-97

TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



LEAD 1 - GATE
LEAD 2 - COLLECTOR
LEAD 3 - SOURCE
TERM. 4 - COLLECTOR

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

NORTH AMERICA
Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

EUROPE
Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

HARRIS SEMICONDUCTOR