



New Product

Si4914DY
Vishay Siliconix

Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
Channel-1	30	0.023 at V _{GS} = 10 V	7.0
		0.032 at V _{GS} = 4.5 V	5.6
Channel-2		0.020 at V _{GS} = 10 V	7.4
		0.027 at V _{GS} = 4.5 V	6.4

SCHOTTKY PRODUCT SUMMARY

V _{DS} (V)	V _{SD} (V) Diode Forward Voltage	I _F (A)
30	0.40 V at 1.0 A	2.0

FEATURES

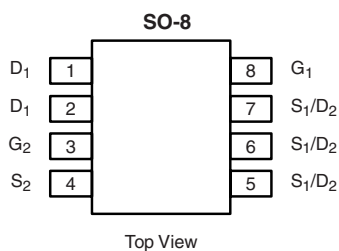
- LITTLE FOOT® Plus Integrated Schottky
- 100 % R_g Tested

APPLICATIONS

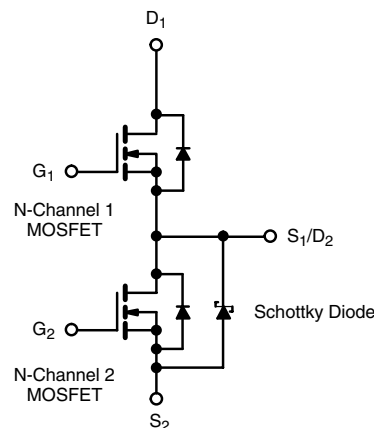
- Logic DC/DC
- Notebook PC



RoHS
COMPLIANT



Ordering Information: Si4914DY-T1-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Channel-1		Channel-2		Unit
			10 sec	Steady State	10 sec	Steady State	
Drain-Source Voltage		V _{DS}	30				V
Gate-Source Voltage		V _{GS}	20				
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	7.0	5.5	7.4	5.7	A
	T _A = 70 °C		5.6	4.3	6	4.5	
Pulsed Drain Current		I _{DM}	40		40		
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	1.0	1.8	0.95	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	13		15		
Avalanche Energy		E _{AS}	8.45		11		mJ
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	1.9	1.1	2.0	1.16	W
	T _A = 70 °C		1.2	0.71	1.3	0.74	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Channel-1		Channel-2		Unit
		Typ	Max	Typ	Max	
Maximum Junction-to-Ambient ^a	R _{thJA}	52	65	47	60	°C/W
		90	112	85	107	
Maximum Junction-to-Foot (Drain)	R _{thJF}	30	38	28	35	

Notes:

a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min	Typ ^a	Max	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	Ch-1	1.0		2.5	V
			Ch-2	1.0		2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = 20\text{ V}$	Ch-1			100	nA
			Ch-2			100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$	Ch-1			1	μA
			Ch-2			500	
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$	Ch-1			0.015	mA
			Ch-2			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}$, $V_{GS} = 10\text{ V}$	Ch-1	20			A
			Ch-2	20			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 7.0\text{ A}$	Ch-1		0.019	0.023	Ω
		$V_{GS} = 10\text{ V}$, $I_D = 7.4\text{ A}$	Ch-2		0.016	0.020	
		$V_{GS} = 4.5\text{ V}$, $I_D = 5.6\text{ A}$	Ch-1		0.026	0.032	
		$V_{GS} = 4.5\text{ V}$, $I_D = 6.4\text{ A}$	Ch-2		0.022	0.027	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 7.0\text{ A}$	Ch-1		19		S
		$V_{DS} = 15\text{ V}$, $I_D = 7.4\text{ A}$	Ch-2		22		
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-1		0.75	1.1	V
		$I_S = 1\text{ A}$, $V_{GS} = 0\text{ V}$	Ch-2		0.36	0.40	
Dynamic ^a							
Total Gate Charge	Q_g	Channel-1 $V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 7.0\text{ A}$	Ch-1		5.6	8.5	nC
			Ch-2		7.3	11	
Gate-Source Charge	Q_{gs}		Ch-1		2.3		
			Ch-2		2.8		
Gate-Drain Charge	Q_{gd}	Channel-2 $V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 7.4\text{ A}$	Ch-1		1.7		
			Ch-2		2.2		
Gate Resistance	R_g		Ch-1	0.5	2.3	3.6	Ω
			Ch-2	0.5	1.6	2.5	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$	Ch-1		6	10	ns
Rise Time	t_r		Ch-2		7	11	
			Ch-1		13	20	
			Ch-2		13	20	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$, $R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$	Ch-1		27	40	
			Ch-2		35	53	
Fall Time	t_f		Ch-1		9	15	
			Ch-2		10	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Ch-1		30	50	
		$I_F = 2.2\text{ A}$, $di/dt = 100\text{ }\mu\text{A}/\mu\text{s}$	Ch-2		30	50	

Notes:

a. Guaranteed by design, not subject to production testing.

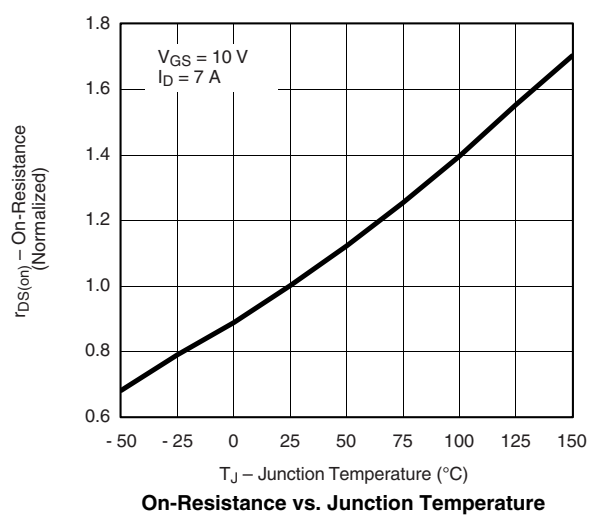
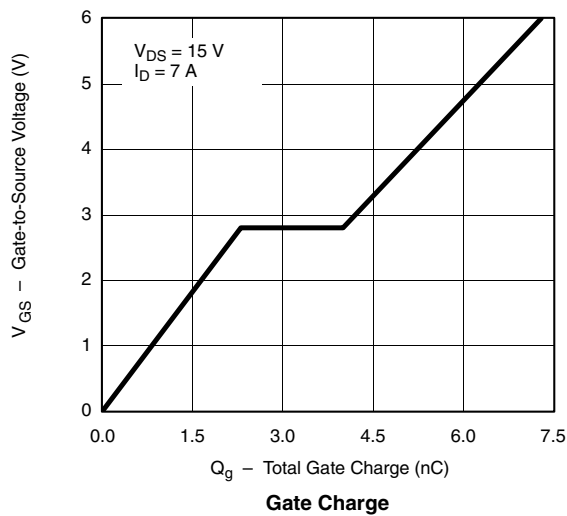
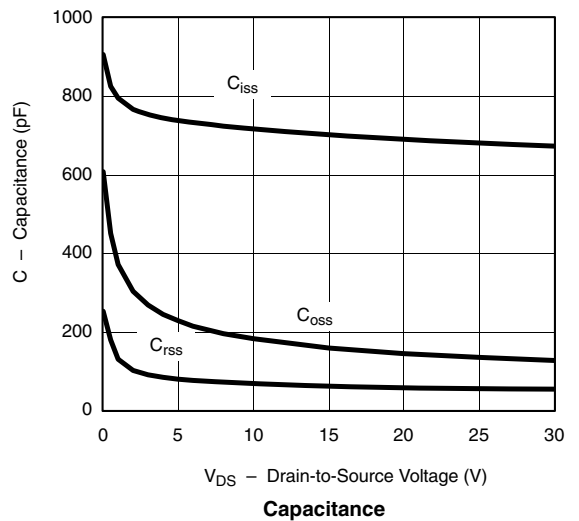
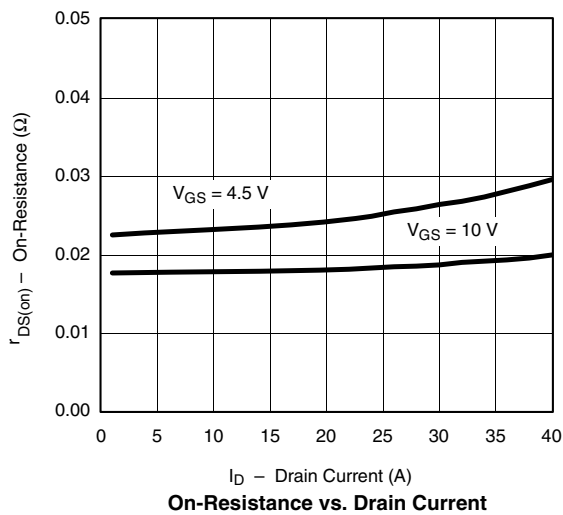
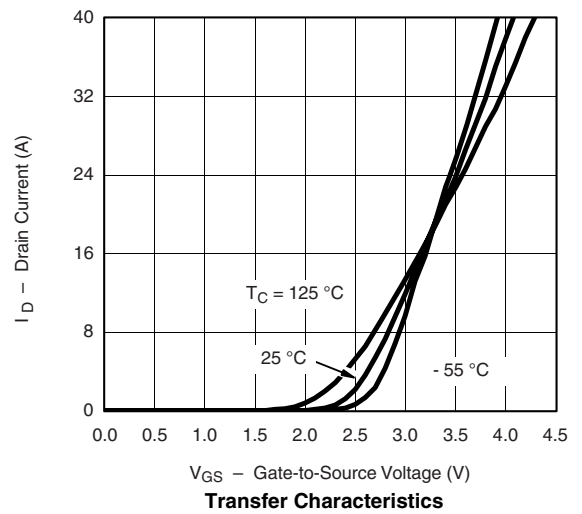
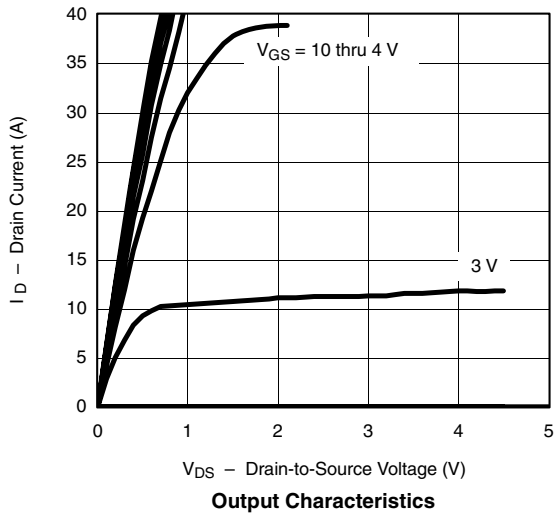
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

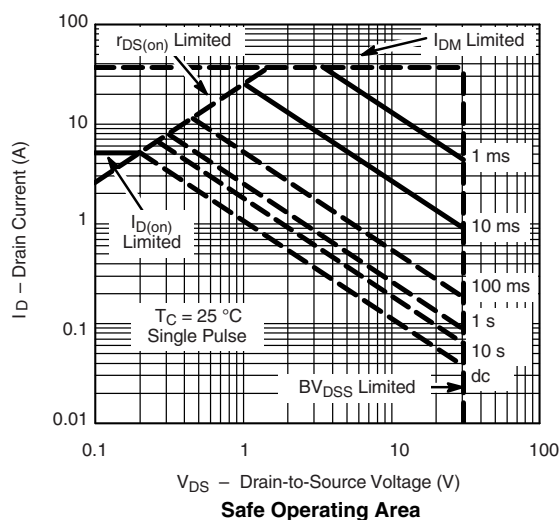
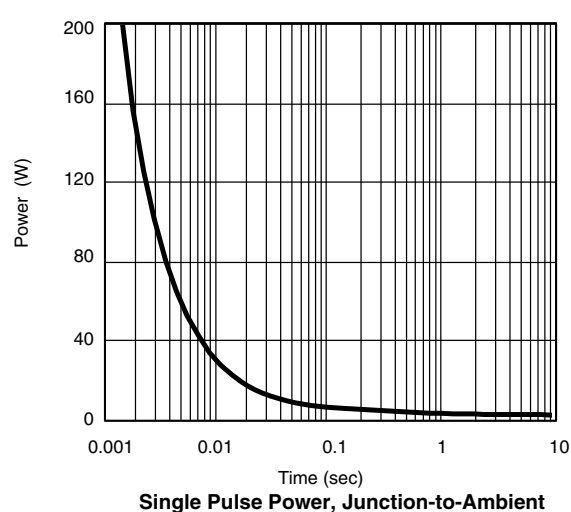
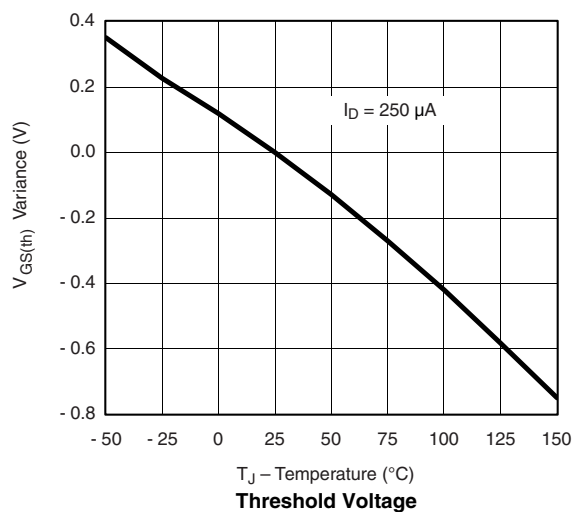
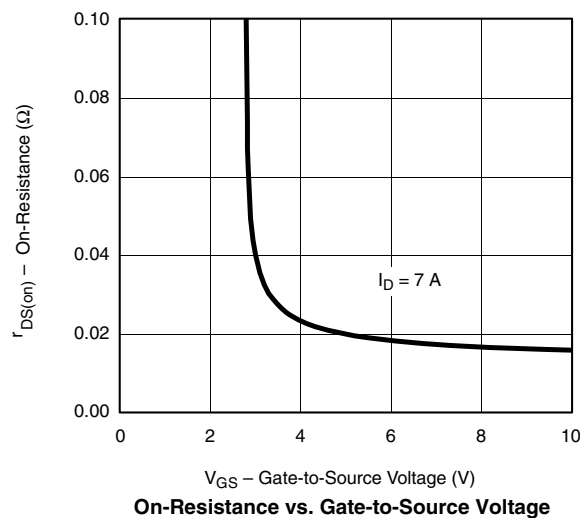
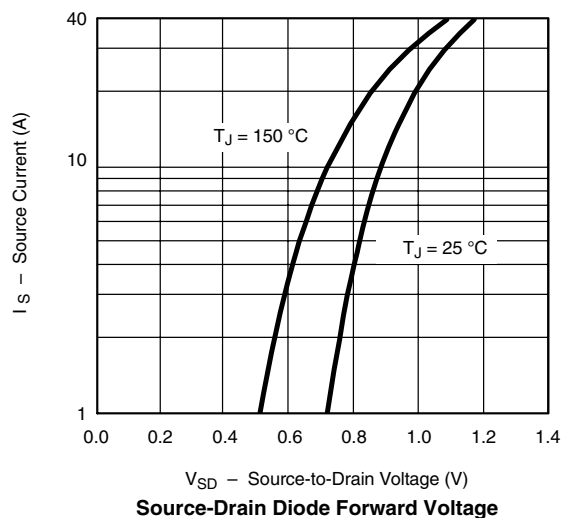
SCHOTTKY SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Forward Voltage Drop	V_F	$I_F = 1.0\text{ A}$		0.36	0.40	V
		$I_F = 1.0\text{ A}$, $T_J = 150\text{ }^{\circ}\text{C}$		0.27	0.31	
Maximum Reverse Leakage Current	I_{rm}	$V_r = 30\text{ V}$		0.008	0.50	mA
		$V_r = 30\text{ V}$, $T_J = 100\text{ }^{\circ}\text{C}$		3.5	10	
		$V_r = -30\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		10	100	
Junction Capacitance	C_T	$V_r = 10\text{ V}$		58		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



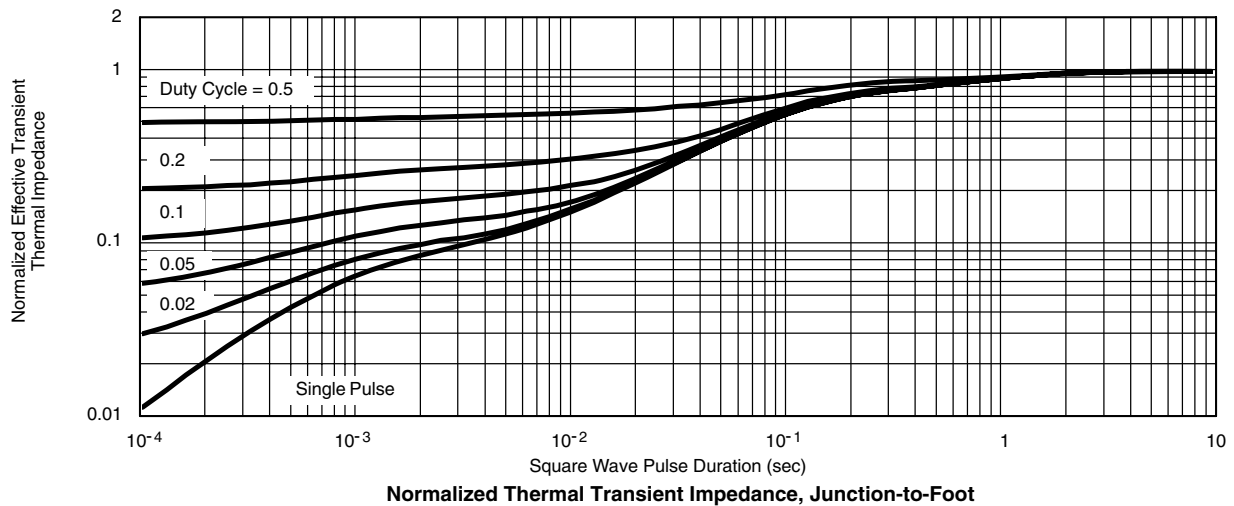
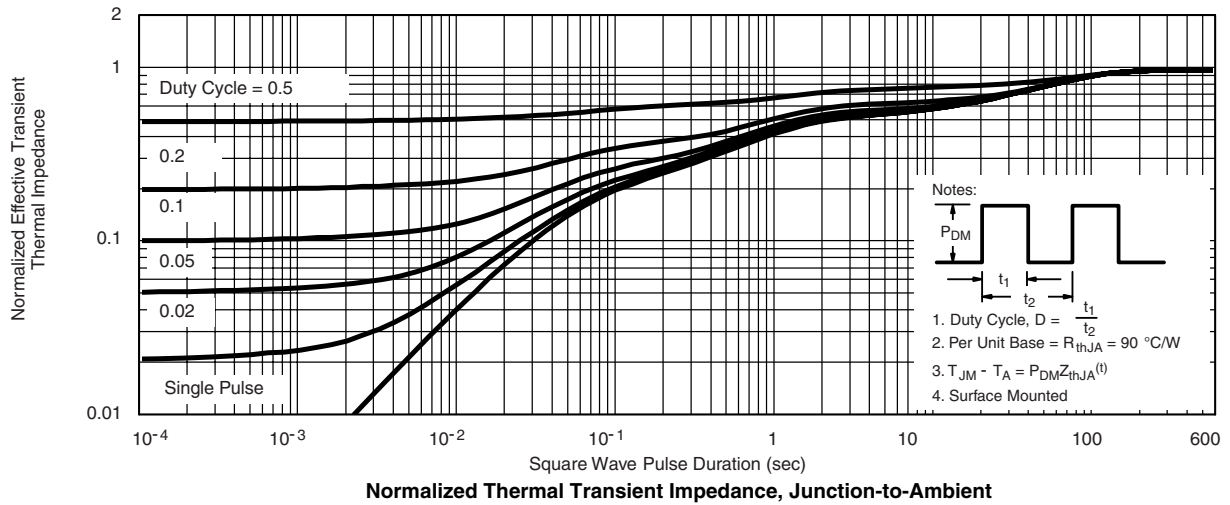
CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless noted

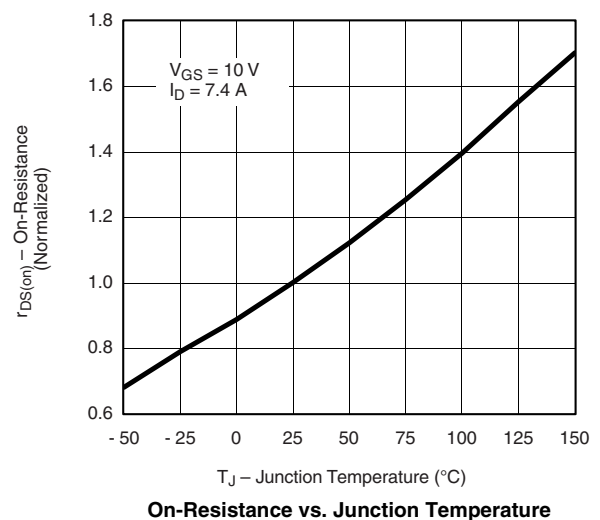
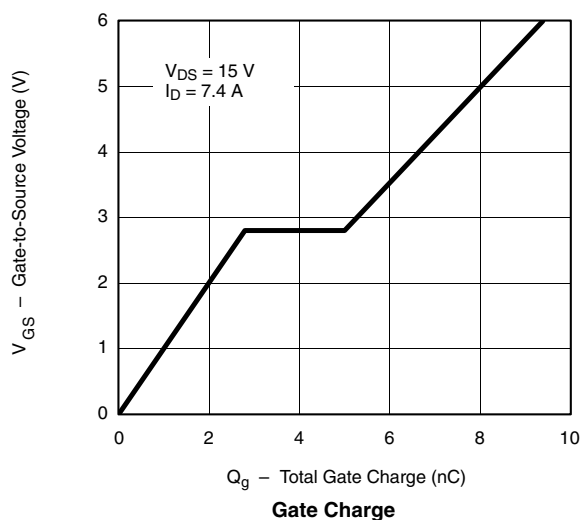
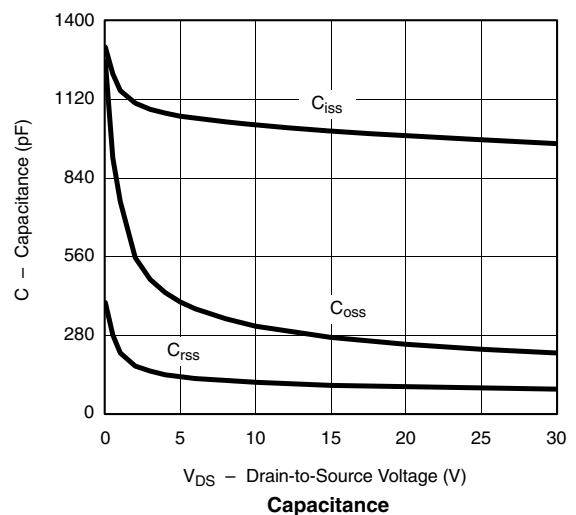
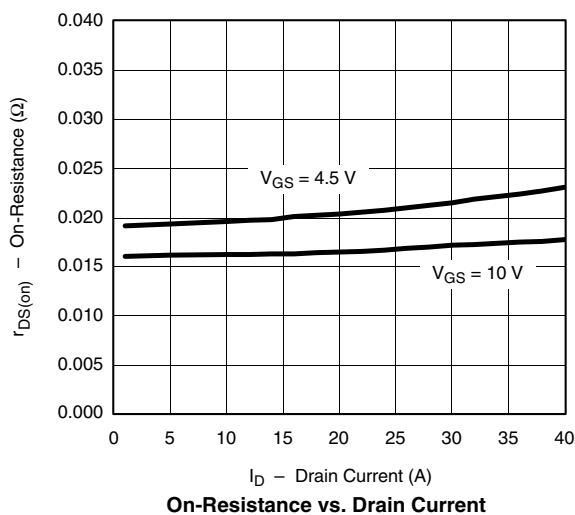
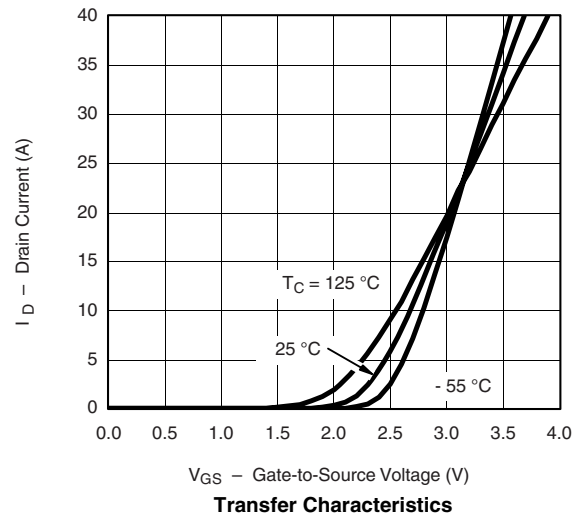
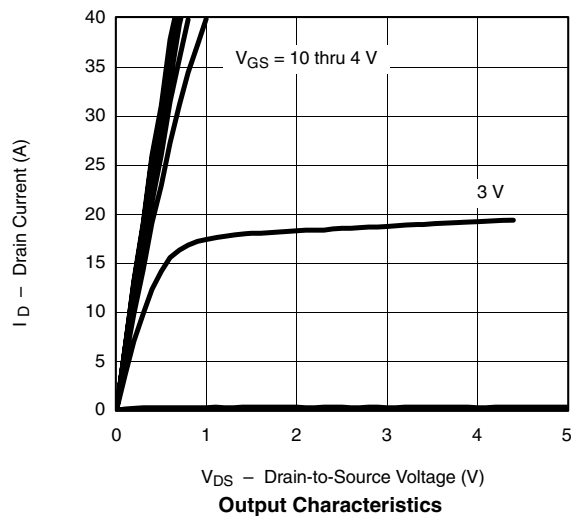


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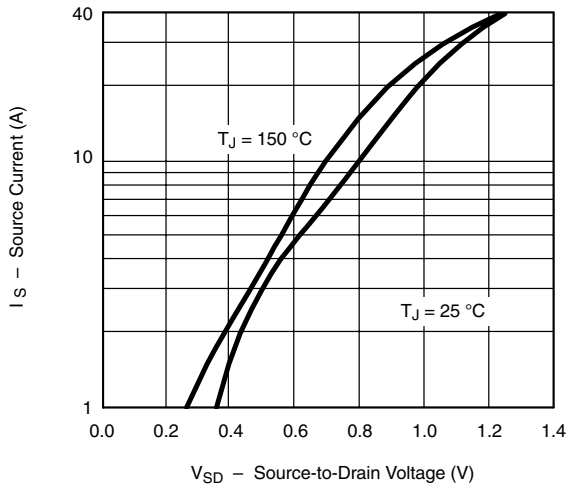
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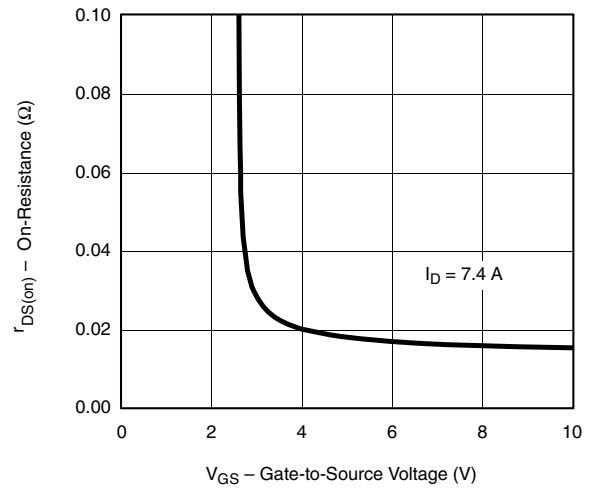
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless noted



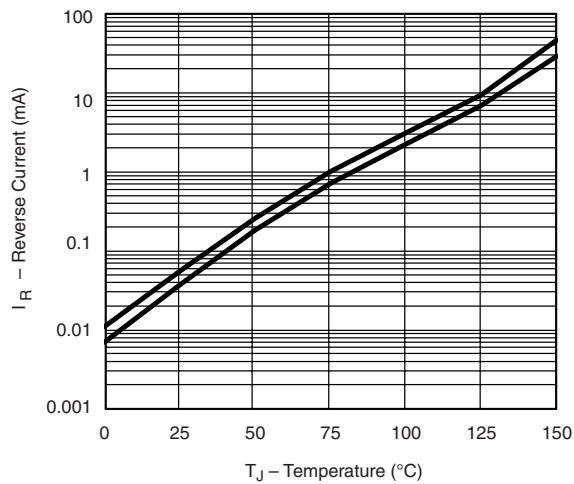
CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless noted



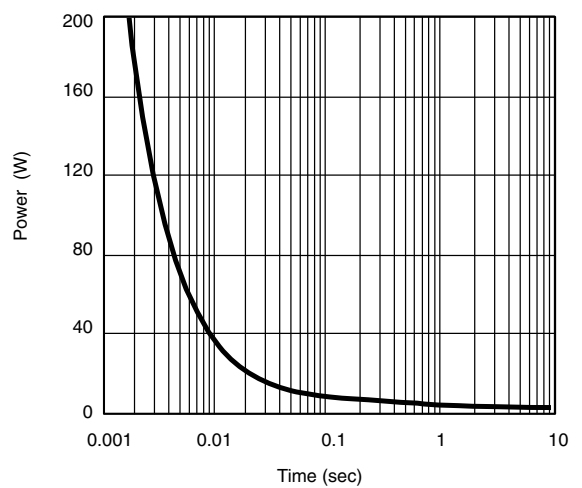
Source-Drain Diode Forward Voltage



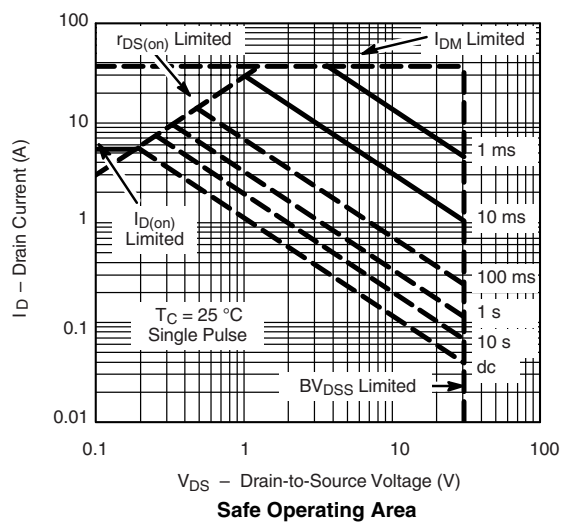
On-Resistance vs. Gate-to-Source Voltage

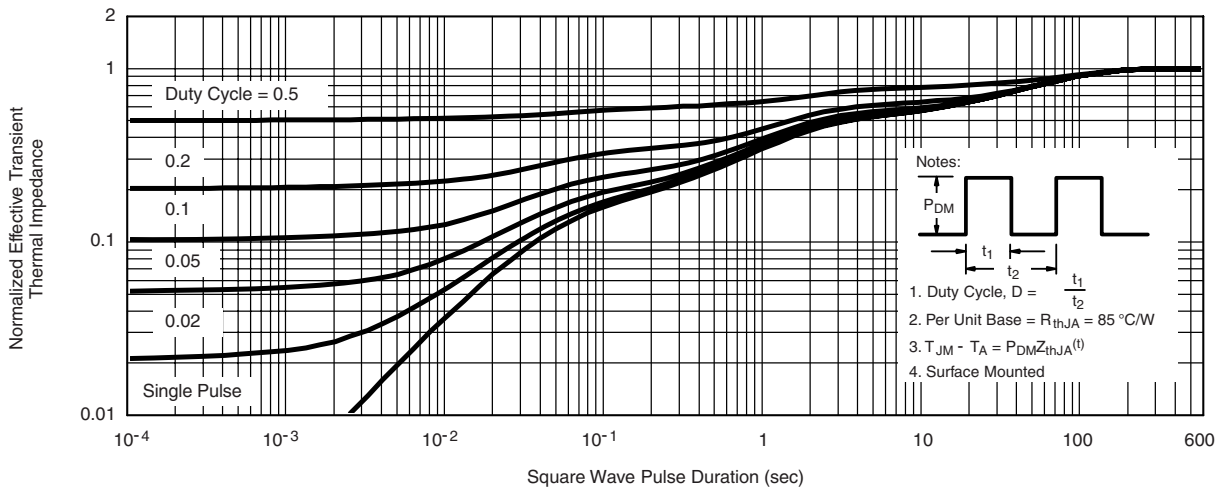
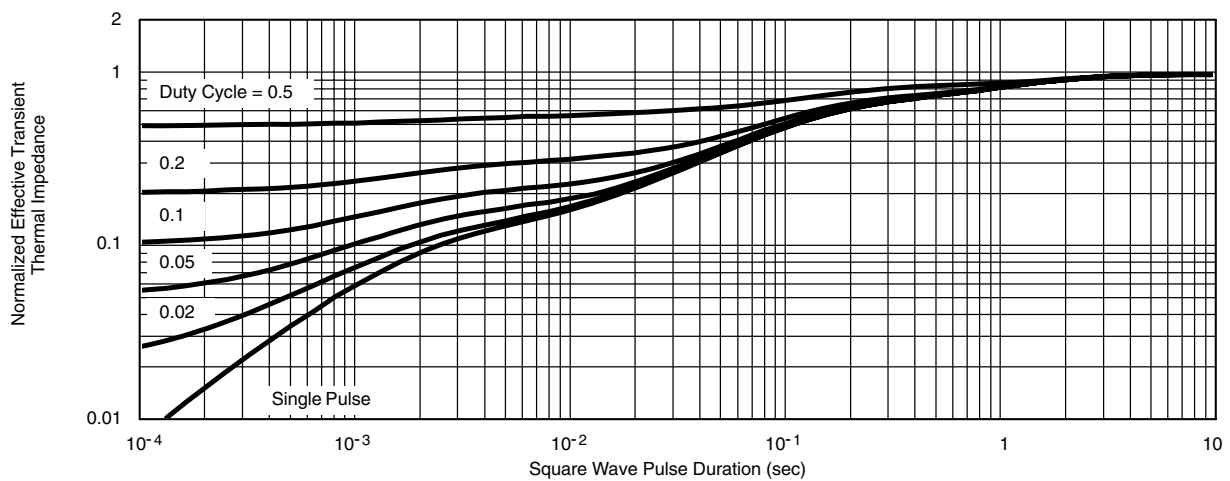


Reverse Current vs. Junction Temperature



Single Pulse Power, Junction-to-Ambient



CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72938>.



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