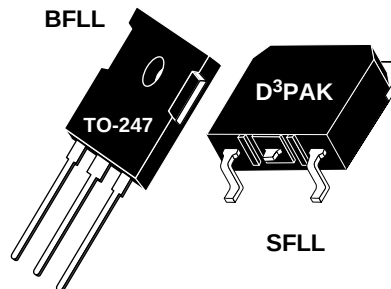
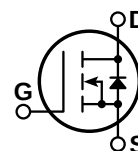


POWER MOS 7™
FREDFET
BFLL

SFLL


Power MOS 7™ is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7™ by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7™ combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package
- **FAST RECOVERY BODY DIODE**

MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT6025	UNIT
V_{DSS}	Drain-Source Voltage	600	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	24	Amps
I_{DM}	Pulsed Drain Current ^①	96	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	325	Watts
	Linear Derating Factor	2.60	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	24	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	600			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	24			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.250	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	3		5	Volts


CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>
USA

405 S.W. Columbia Street

Bend, Oregon 97702-1035

Phone: (541) 382-8028

FAX: (541) 388-0364

EUROPE

Chemin de Magret

F-33700 Merignac - France

Phone: (33) 5 57 92 15 15

FAX: (33) 5 56 47 97 61

APT6025 BFLL - SFLL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1 MHz		2730		pF
C _{oss}	Output Capacitance			480		
C _{rss}	Reverse Transfer Capacitance			31		
Q _g	Total Gate Charge ③	V _{GS} = 10V V _{DD} = 0.5 V _{DSS} I _D = I _D [Cont.] @ 25°C		63		nC
Q _{gs}	Gate-Source Charge			15		
Q _{gd}	Gate-Drain ("Miller") Charge			28		
t _{d(on)}	Turn-on Delay Time	V _{GS} = 15V V _{DD} = 0.5 V _{DSS} I _D = I _D [Cont.] @ 25°C R _G = 1.6Ω		13		ns
t _r	Rise Time			8		
t _{d(off)}	Turn-off Delay Time			30		
t _f	Fall Time			8		

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			24	Amps
I_{SM}	Pulsed Source Current ^① (Body Diode)			96	
V_{SD}	Diode Forward Voltage ^② ($V_{GS} = 0V$, $I_S = -I_D$ [Cont.])			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			15	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D$ [Cont.], $di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		250	ns
		$T_j = 125^\circ C$		525	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D$ [Cont.], $di/dt = 100A/\mu s$)	$T_j = 25^\circ C$	1.5		μC
		$T_j = 125^\circ C$	5.5		
I_{RRM}	Peak Recovery Current ($I_S = -I_D$ [Cont.], $di/dt = 100A/\mu s$)	$T_j = 25^\circ C$	13		Amps
		$T_j = 125^\circ C$	23		

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.38	°C/W
R _{θJA}	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μ s, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ\text{C}$, $L = 4.51\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 24\text{A}$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_{H(Cont)}$ $dI/dt \leq 700\text{A}/\mu\text{s}$ $V_P \leq V_{DSS}$ $T_J \leq 150^\circ\text{C}$

APT Reserves the right to change, without notice, the specifications and information contained herein.

D³PAK Package Outline

