

FDD16AN08A0

N-Channel UltraFET® Trench MOSFET 75V, 50A, 16mΩ

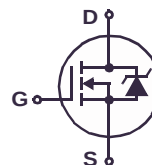
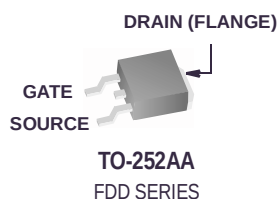
Features

- $r_{DS(ON)} = 13\text{m}\Omega$ (Typ.), $V_{GS} = 10\text{V}$, $I_D = 50\text{A}$
- $Q_g(\text{tot}) = 31\text{nC}$ (Typ.), $V_{GS} = 10\text{V}$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101

Formerly developmental type 82660

Applications

- 42V Automotive Load Control
- Starter / Alternator Systems
- Electronic Power Steering Systems
- Electronic Valve Train Systems
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V systems



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	75	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_C < 79^\circ\text{C}$, $V_{GS} = 10\text{V}$)	50	A
	Continuous ($T_{amb} = 25^\circ\text{C}$, $V_{GS} = 10\text{V}$, with $R_{\theta JA} = 52^\circ\text{C/W}$)	9	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	95	mJ
P_D	Power dissipation	135	W
	Derate above 25°C	0.9	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252	1.11	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in ² copper pad area	52	$^\circ\text{C/W}$

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD16AN08A0	FDD16AN08A0	TO-252AA	330mm	16mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	75	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1 250	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 50\text{A}$, $V_{GS} = 10\text{V}$	-	0.013	0.016	Ω
		$I_D = 25\text{A}$, $V_{GS} = 6\text{V}$	-	0.019	0.029	
		$I_D = 50\text{A}$, $V_{GS} = 10\text{V}$, $T_J = 175^\circ\text{C}$	-	0.032	0.037	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	1874	-	pF
C_{OSS}	Output Capacitance		-	290	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	91	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V		31	47	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 2V		4	6	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 40\text{V}$ $I_D = 50\text{A}$ $I_g = 1.0\text{mA}$	-	9.7	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	5.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	7.2	-	nC
			-			

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 40\text{V}$, $I_D = 50\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 10\Omega$	-	-	93	ns
$t_{d(ON)}$	Turn-On Delay Time		-	8	-	ns
t_r	Rise Time		-	54	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	32	-	ns
t_f	Fall Time		-	22	-	ns
t_{OFF}	Turn-Off Time		-	-	81	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 50\text{A}$	-	-	1.25	V
		$I_{SD} = 25\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 50\text{A}$, $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	34	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 50\text{A}$, $di_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	31	nC

Notes:

1: Starting $T_J = 25^\circ\text{C}$, $L = 155\mu\text{H}$, $I_{AS} = 35\text{A}$.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

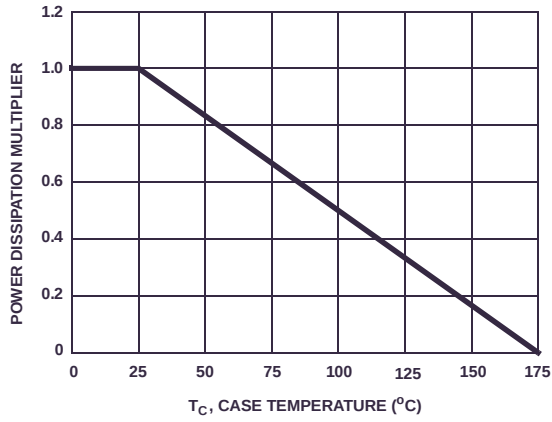


Figure 1. Normalized Power Dissipation vs Ambient Temperature

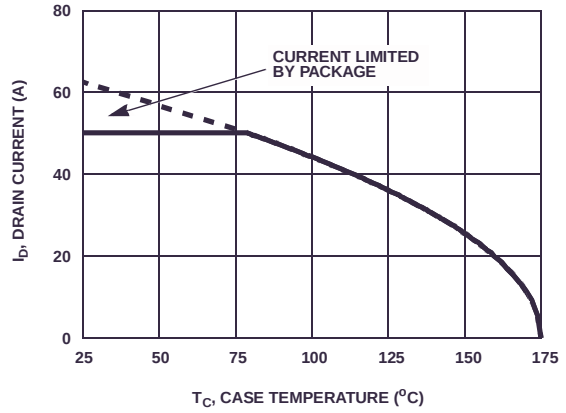


Figure 2. Maximum Continuous Drain Current vs Case Temperature

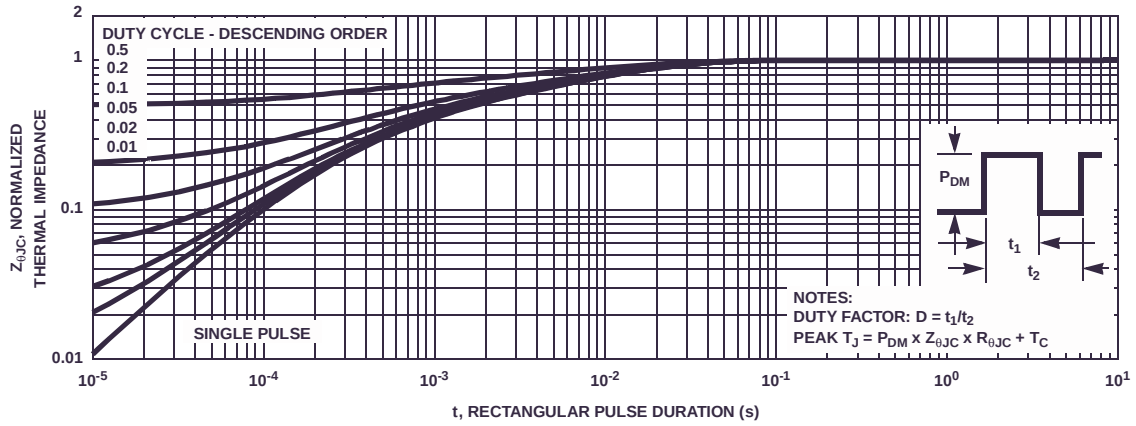


Figure 3. Normalized Maximum Transient Thermal Impedance

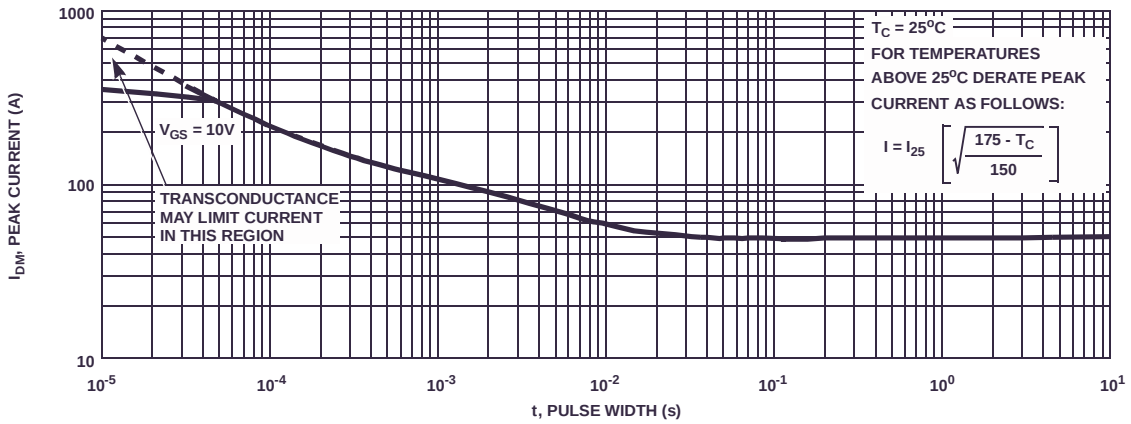


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

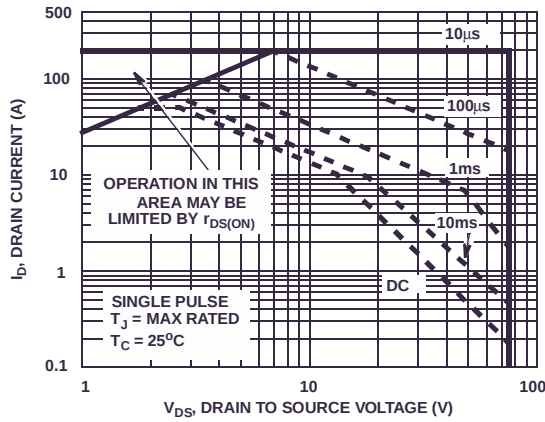
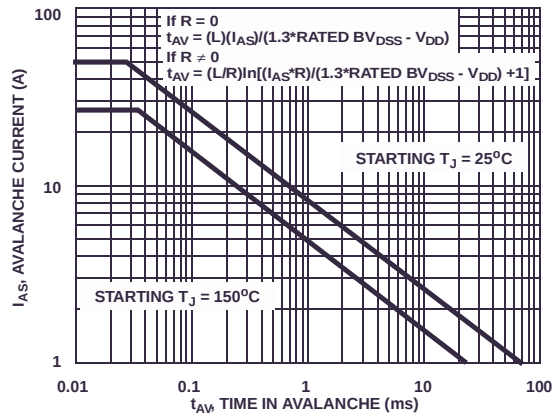


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
Figure 6. Unclamped Inductive Switching Capability

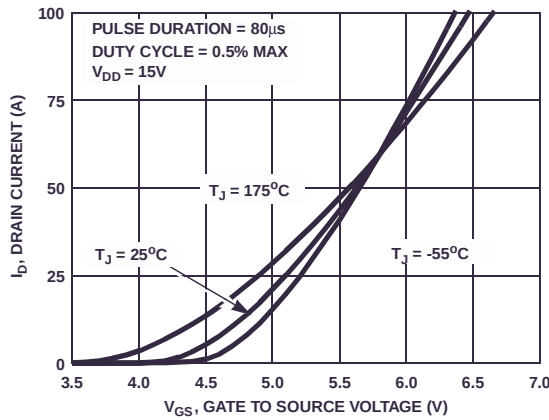


Figure 7. Transfer Characteristics

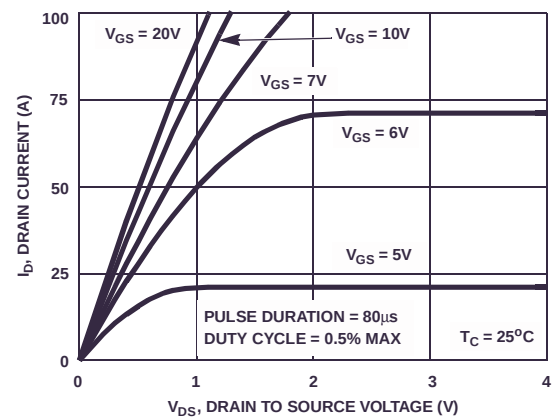


Figure 8. Saturation Characteristics

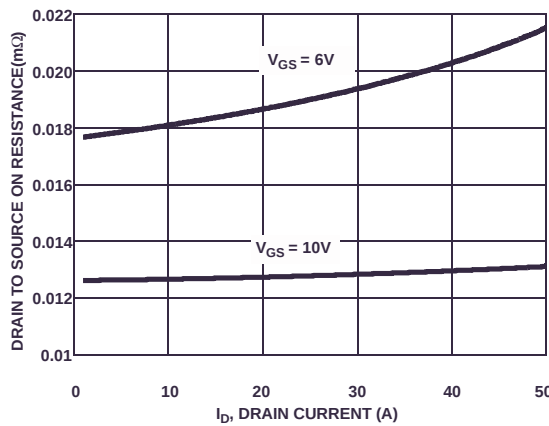


Figure 9. Drain to Source On Resistance vs. Drain Current

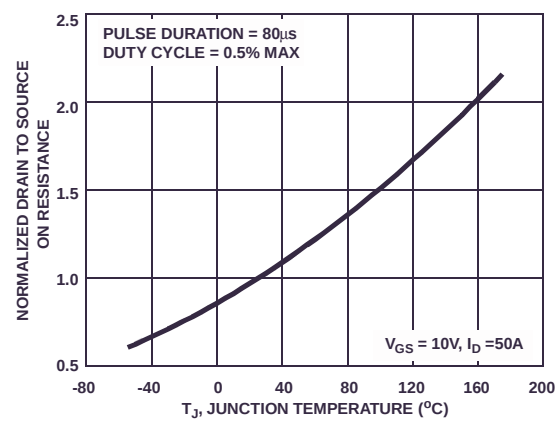


Figure 10. Normalized Drain to Source On Resistance vs. Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

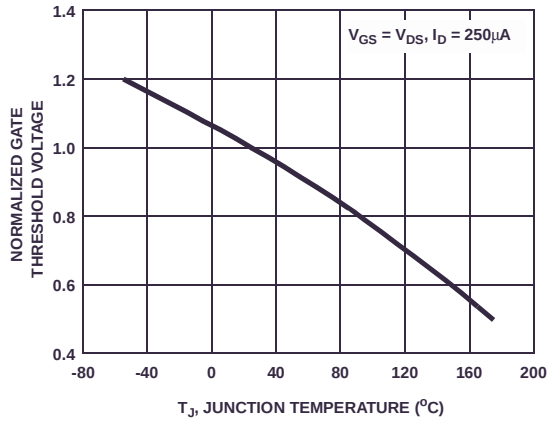


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

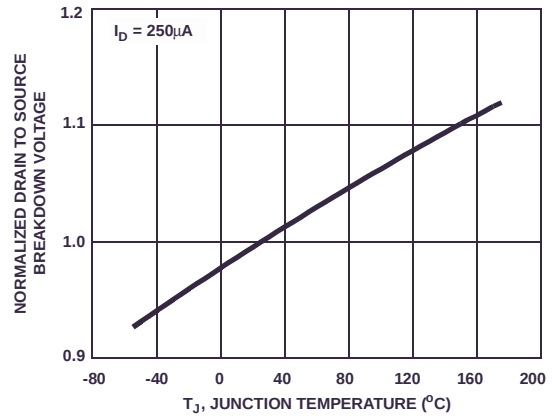


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

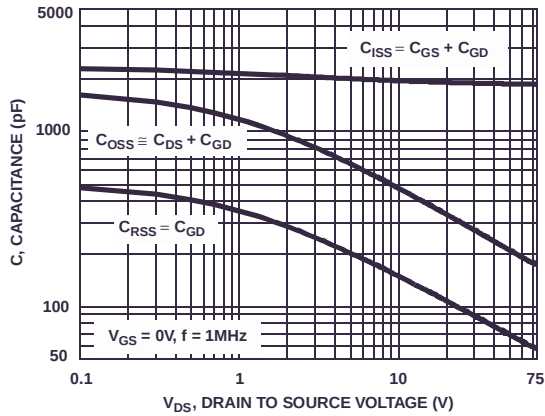


Figure 13. Capacitance vs Drain to Source Voltage

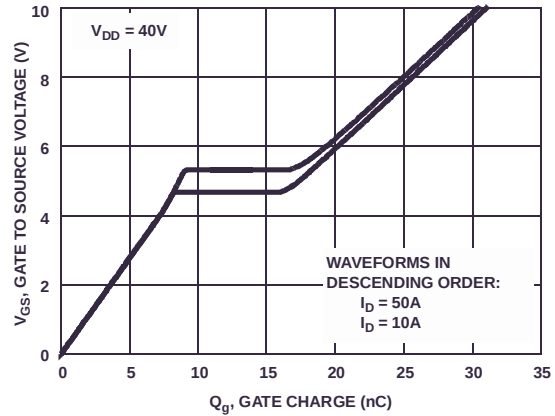


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

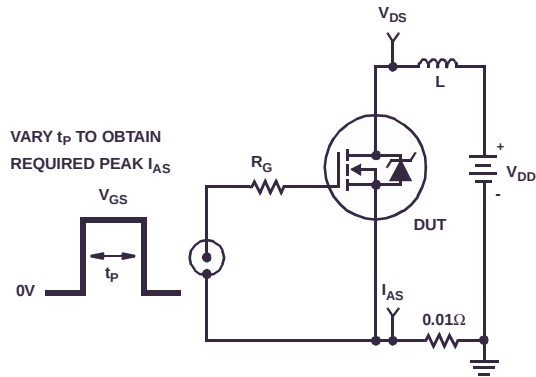


Figure 15. Unclamped Energy Test Circuit

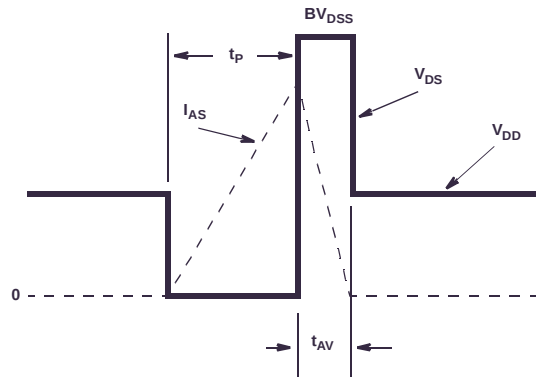


Figure 16. Unclamped Energy Waveforms

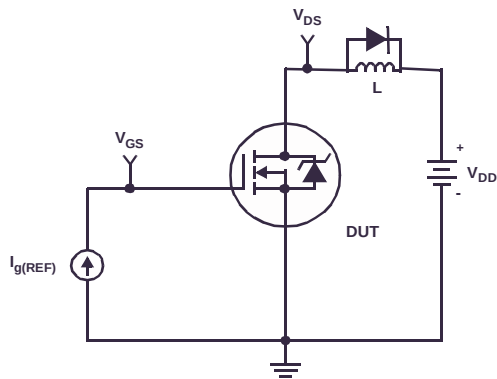


Figure 17. Gate Charge Test Circuit

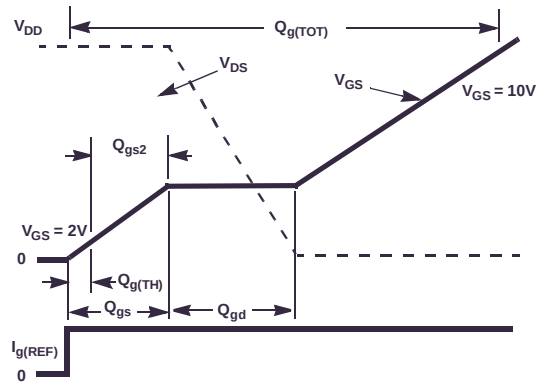


Figure 18. Gate Charge Waveforms

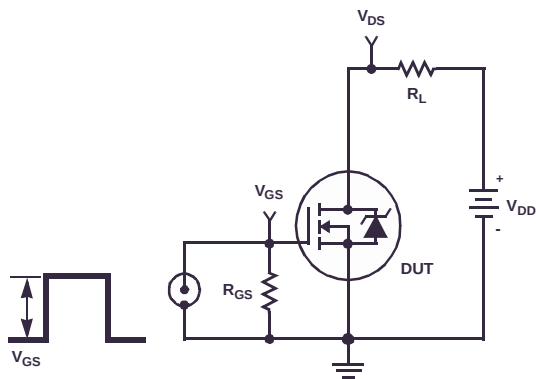


Figure 19. Switching Time Test Circuit

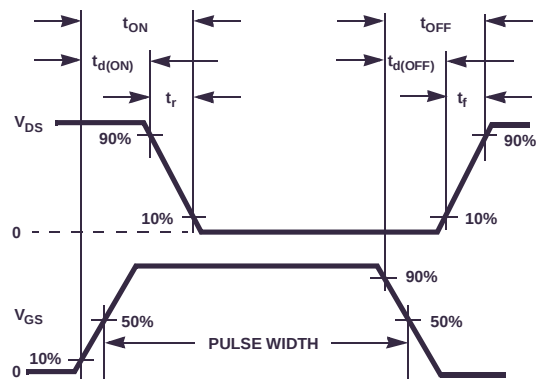


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}\text{C}$), and thermal resistance $R_{\theta JA}$ ($^{\circ}\text{C/W}$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + \text{Area})} \quad (\text{EQ. 2})$$

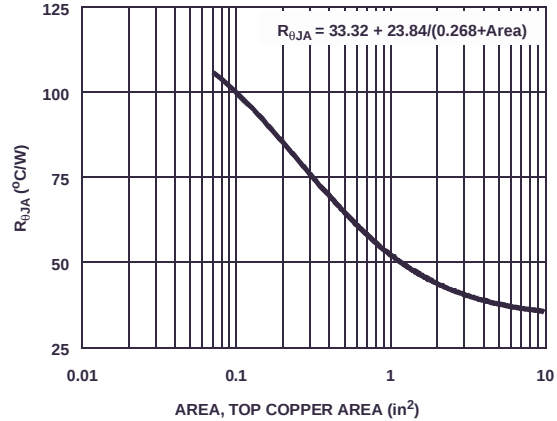


Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

.SUBCKT FDD16AN08A0 2 1 3 ; rev March 2002

Ca 12 8 6.8e-10
Cb 15 14 8.9e-10
Cin 6 8 1.8e-9

Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 80.00
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Etemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 4.81e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 4.63e-9

RLgate 1 9 48.1
RLdrain 2 5 10
RLsource 3 7 46.3

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 2e-3
Rgate 9 20 3.9
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 7e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*200),3))}}

.MODEL DbodyMOD D (IS=2.4E-11 N=1.08 RS=3.6e-3 TRS1=2.2e-3 TRS2=2.5e-9
+ CJO=1.2e-9 M=5.4e-1 TT=1.70e-8 XTI=3.9)

.MODEL DbreakMOD D (RS=1.5e-1 TRS1=1e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=0.5e-9 IS=1e-30 N=10 M=0.5)

.MODEL MmedMOD NMOS (VTO=3.65 KP=3 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=3.9)

.MODEL MstroMOD NMOS (VTO=4.1 KP=67 IS=1e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=3.05 KP=0.06 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=39 RS=0.1)

.MODEL RbreakMOD RES (TC1=0.9e-3 TC2=-5e-7)

.MODEL RdrainMOD RES (TC1=2.5e-2 TC2=6.2e-5)

.MODEL RSLCMOD RES (TC1=1e-3 TC2=1e-5)

.MODEL RsourceMOD RES (TC1=1e-3 TC2=1e-6)

.MODEL RvthresMOD RES (TC1=-5.3e-3 TC2=-1.3e-5)

.MODEL RvtempMOD RES (TC1=-2.7e-3 TC2=1e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-1.5)

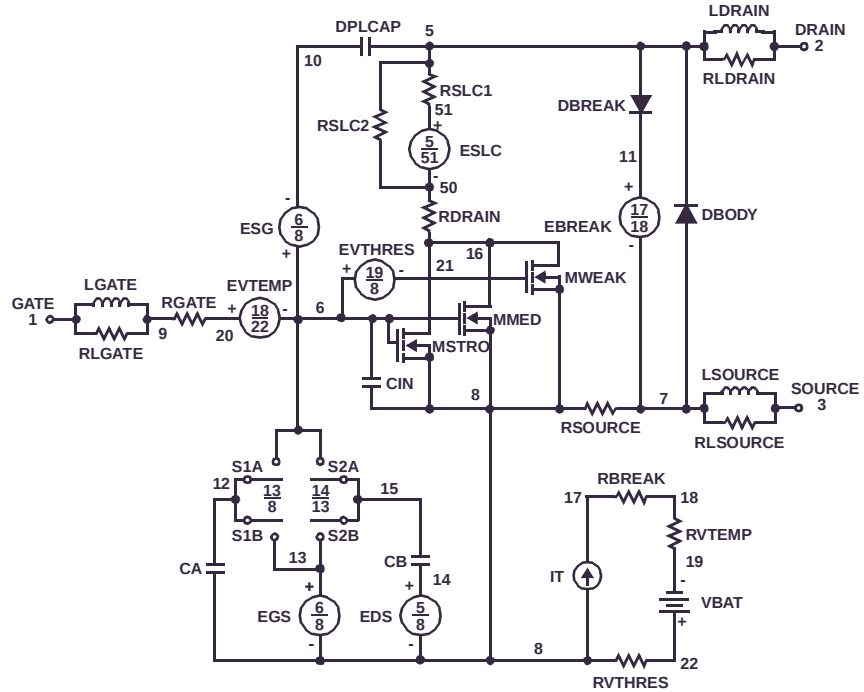
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-4)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=0.5)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-1)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



PSPICE Thermal Model

REV 23 March 2002

FDD16AN08A0T

CTHERM1 th 6 0.002
CTHERM2 6 5 0.004
CTHERM3 5 4 0.006
CTHERM4 4 3 0.01
CTHERM5 3 2 0.03
CTHERM6 2 tl 0.08

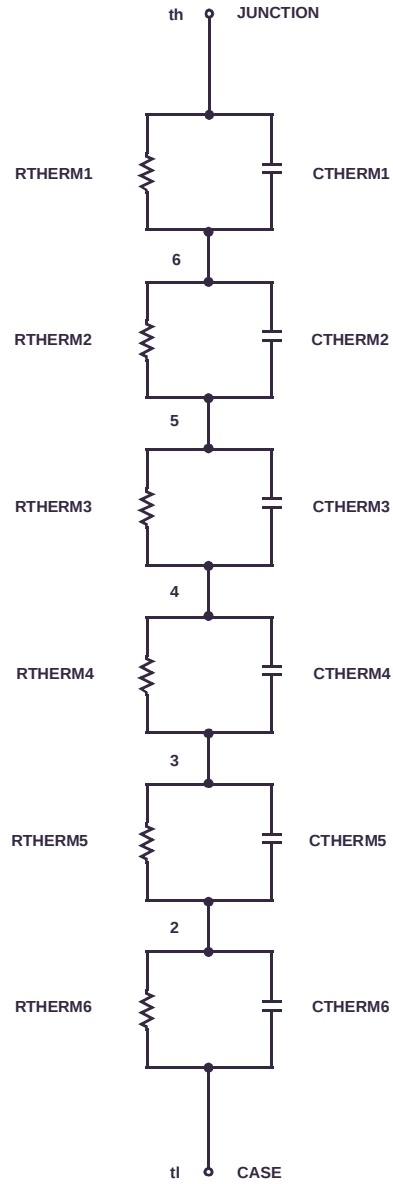
RTHERM1 th 6 0.075
RTHERM2 6 5 0.09
RTHERM3 5 4 0.1
RTHERM4 4 3 0.15
RTHERM5 3 2 0.2
RTHERM6 2 tl 0.25

SABER Thermal Model

SABER thermal model FDD16AN08A0T
template thermal_model th tl
thermal_c th, tl

```
{
  ctherm.ctherm1 th 6 = 0.002
  ctherm.ctherm2 6 5 = 0.004
  ctherm.ctherm3 5 4 = 0.006
  ctherm.ctherm4 4 3 = 0.01
  ctherm.ctherm5 3 2 = 0.03
  ctherm.ctherm6 2 tl = 0.08
```

```
  rtherm.rtherm1 th 6 = 0.075
  rtherm.rtherm2 6 5 = 0.09
  rtherm.rtherm3 5 4 = 0.1
  rtherm.rtherm4 4 3 = 0.15
  rtherm.rtherm5 3 2 = 0.2
  rtherm.rtherm6 2 tl = 0.25
}
```



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CROSSVOLT™	GTO™	Power247™	SuperSOT™-6
DenseTrench™	HiSeC™	PowerTrench®	SuperSOT™-8
DOME™	I ² C™	QFET™	SyncFET™
EcoSPARK™	ISOPLANAR™	QS™	TinyLogic™
E ² CMOS™	LittleFET™	QT Optoelectronics™	TruTranslation™
EnSigna™	MicroFET™	Quiet Series™	UHC™
FACT™	MicroPak™	SILENT SWITCHER®	UltraFET®
FACT Quiet Series™	MICROWIRE™	SMART START™	VCX™
FAST®	OPTOLOGIC®	SPM™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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