

IRF640, IRF641, IRF642, IRF643, RF1S640, RF1S640SM

**16A and 18A, 150V and 200V, 0.18 and 0.22 Ohm,
 N-Channel Power MOSFETs**

January 1998

Features

- 16A and 18A, 150V and 200V
- $r_{DS(ON)} = 0.18\Omega$ and 0.22Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speed
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

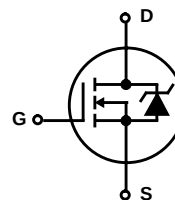
Formerly developmental type TA17422.

Ordering Information

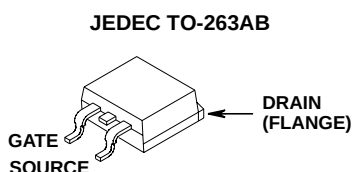
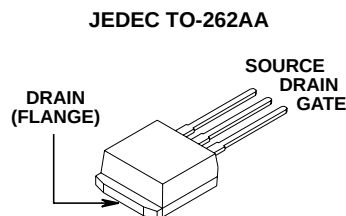
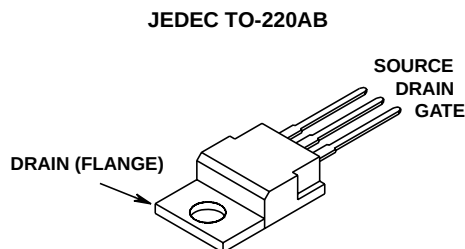
PART NUMBER	PACKAGE	BRAND
IRF640	TO-220AB	IRF640
IRF641	TO-220AB	IRF641
IRF642	TO-220AB	IRF642
IRF643	TO-220AB	IRF643
RF1S640	TO-262AA	RF1S640
RF1S640SM	TO-263AB	RF1S640

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., RF1S640SM9A.

Symbol



Packaging



IRF640, IRF641, IRF642, IRF643, RF1S640, RF1S640SM

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	IRF640, RF1S640, RF1S640SM	IRF641	IRF642	IRF643	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS} 200	150	200	150	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR} 200	150	200	150	V
Continuous Drain Current	I_D 18	18	16	16	A
$T_C = 100^{\circ}\text{C}$	I_D 11	11	10	10	A
Pulsed Drain Current (Note 3)	I_{DM} 72	72	64	64	A
Gate to Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D 125	125	125	125	W
Dissipation Derating Factor	1.0	1.0	1.0	1.0	$\text{W}/^{\circ}\text{C}$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS} 580	580	580	580	mJ
Operating and Storage Temperature	T_J, T_{STG} -55 to 150	-55 to 150	-55 to 150	-55 to 150	$^{\circ}\text{C}$
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s	T_L 300	300	300	300	$^{\circ}\text{C}$
Package Body for 10s, See TB334	T_{pkg} 260	260	260	260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

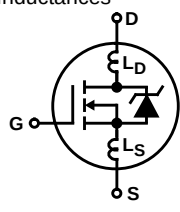
1. $T_J = 25^{\circ}\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

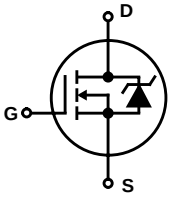
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage IRF640, IRF642, RF1S640, RF1S640SM	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$, (Figure 10)	200	-	-	V
IRF641, IRF643			150	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_J = 125^{\circ}\text{C}$	-	-	250	μA
On-State Drain Current (Note 1) IRF640, IRF641, RF1S640, RF1S640SM	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10\text{V}$, (Figure 7)	18	-	-	A
IRF642, IRF643			16	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
Drain to Source On Resistance (Note 1) IRF640, IRF641, RF1S640, RF1S640SM	$r_{DS(ON)}$	$I_D = 10\text{A}, V_{GS} = 10\text{V}$, (Figures 8, 9)	-	0.14	0.18	Ω
IRF642, IRF643			-	0.20	0.22	Ω
Forward Transconductance (Note 1)	g_{fs}	$V_{DS} \geq 50\text{V}, I_D = 10\text{A}$, (Figure 12)	6.7	10	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 100\text{V}, I_D \approx 18\text{A}, R_{GS} = 9.1\Omega, R_L = 5.4\Omega$, (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	13	21	ns
Rise Time	t_r		-	50	77	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	46	68	ns
Fall Time	t_f		-	35	54	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 10\text{V}, I_D \approx 18\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature $I_{G(REF)} = 1.5\text{mA}$	-	43	64	nC
Gate to Source Charge	Q_{gs}		-	8	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	22	-	nC

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Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz, (Figure 11)		-	1275	-	pF
Output Capacitance	C _{OSS}			-	400	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	100	-	pF
Internal Drain Inductance	L _D	Measured From the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die		-	4.5	-	nH
Internal Source Inductance	L _S	Measured From the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad			-	7.5	-
Thermal Resistance Junction to Case	R _{θJC}			-	-	1	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	Free Air Operation IRF640, IRF641, IRF642, IRF643, RF1S640		-	-	62	°C/W
	R _{θJA}	RF1S640SM Mounted on FR-4 Board with Minimum Mounting Pad		-	-	62	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 		-	-	18	A
Pulse Source to Drain Current (Note 2)	I_{SDM}			-	-	72	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 18\text{A}$, $V_{GS} = 0\text{V}$, (Figure 13)		-	-	2.0	V
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 18\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		120	240	530	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = 18\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		1.3	2.8	5.6	μC

NOTES:

- Pulse Test: Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
- $V_{DD} = 50\text{V}$, starting $T_J = 25^{\circ}\text{C}$, $L = 3.37\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 18\text{A}$. (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

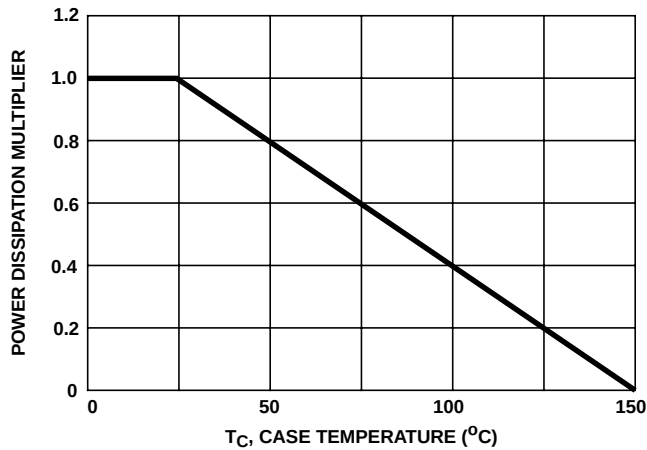


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

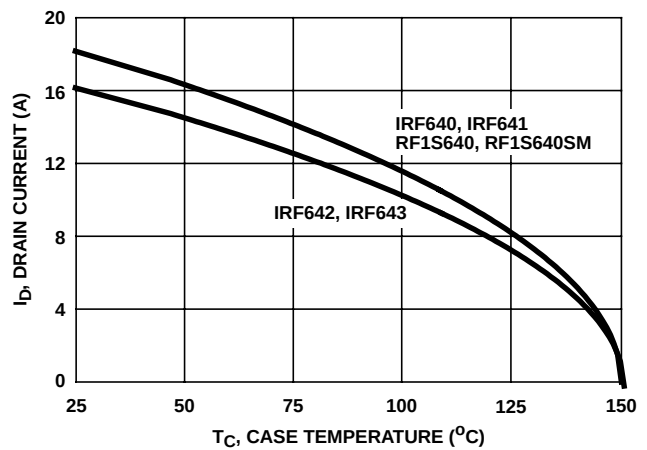


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

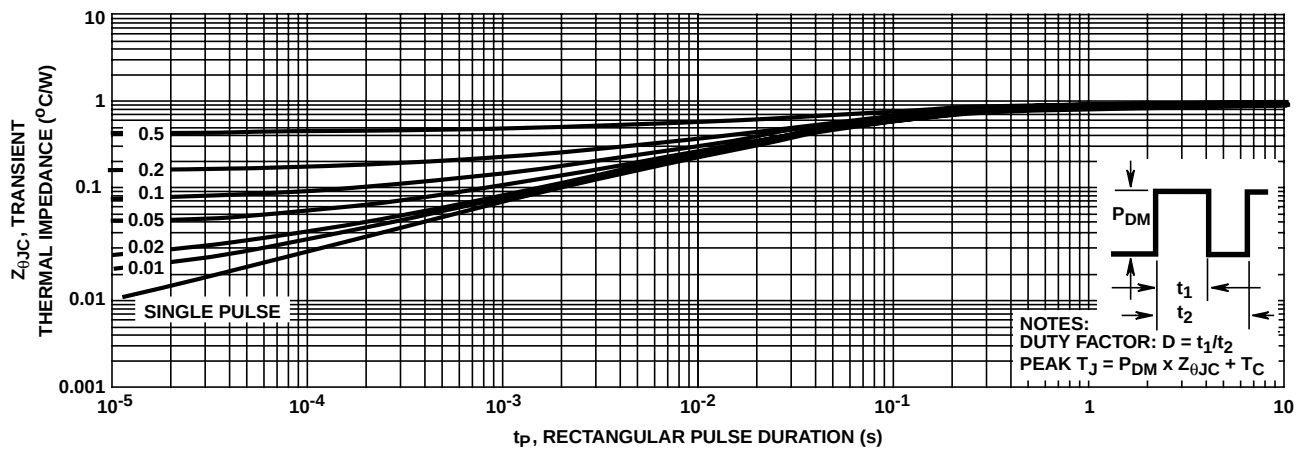


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

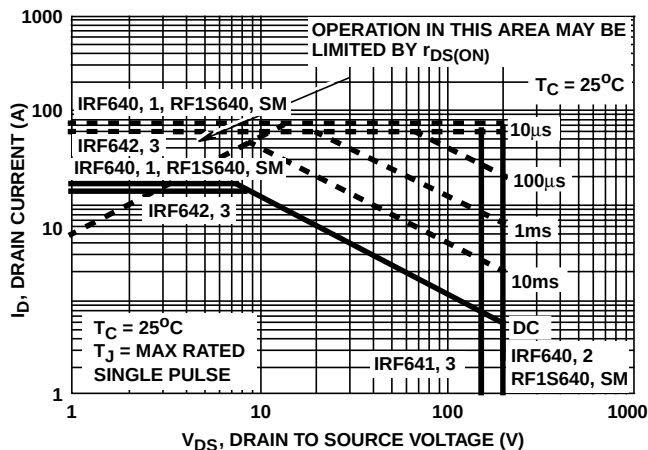


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

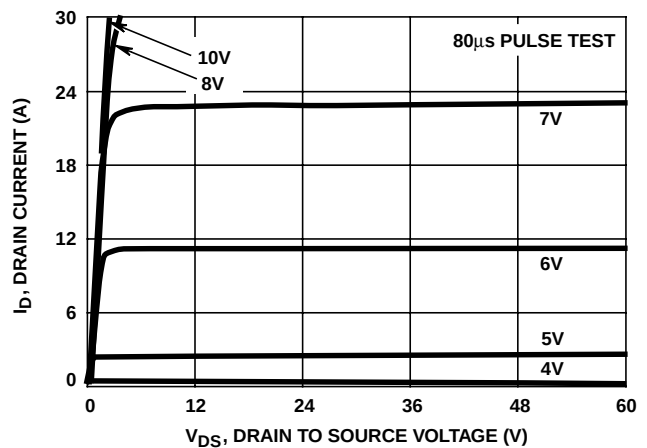


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

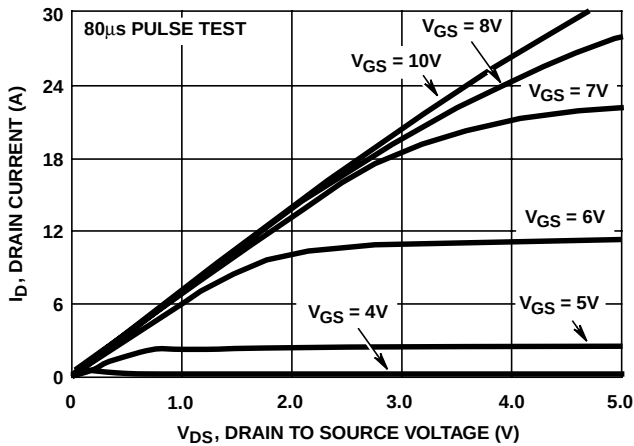


FIGURE 6. SATURATION CHARACTERISTICS

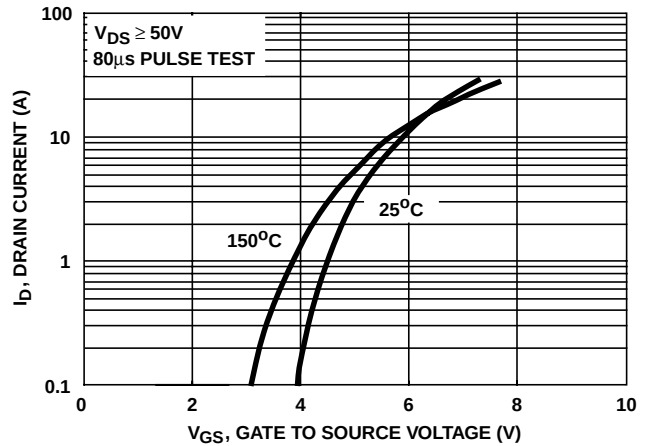


FIGURE 7. TRANSFER CHARACTERISTICS

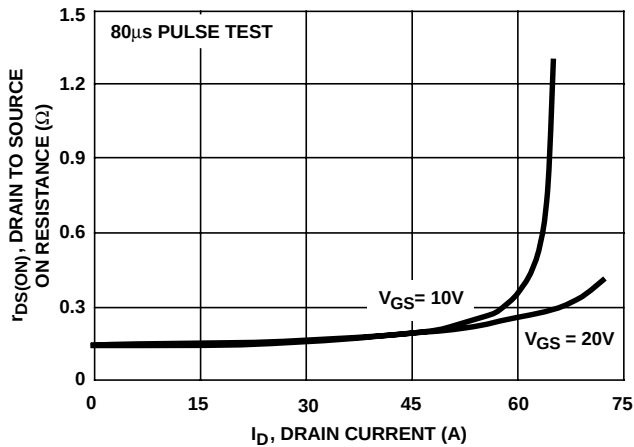


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

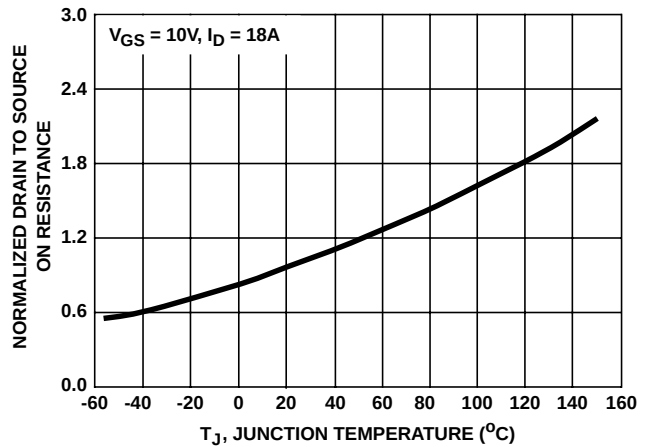


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

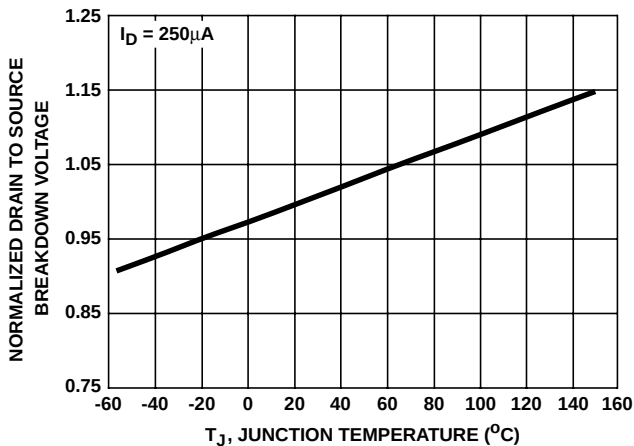


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

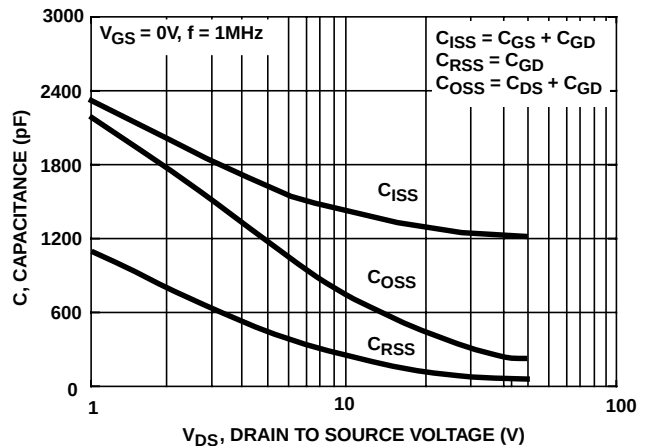


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

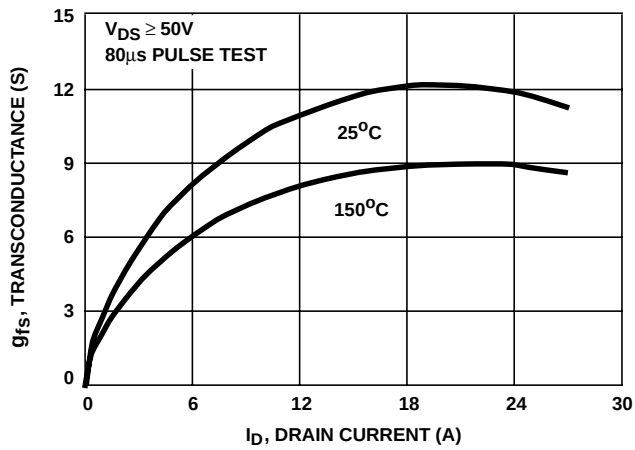


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

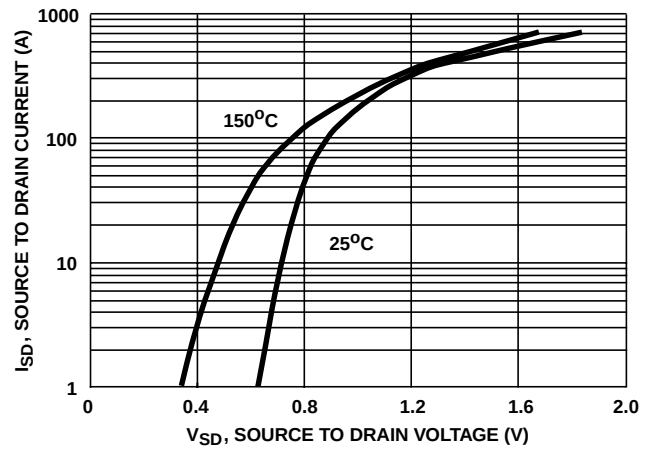


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

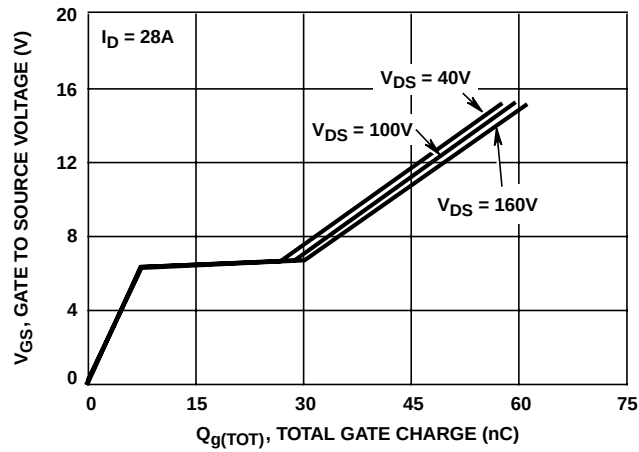


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

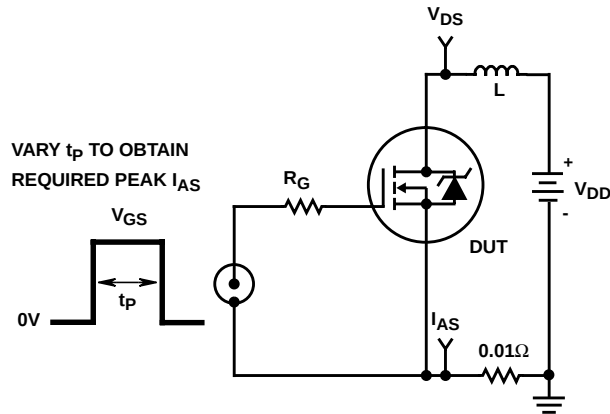


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

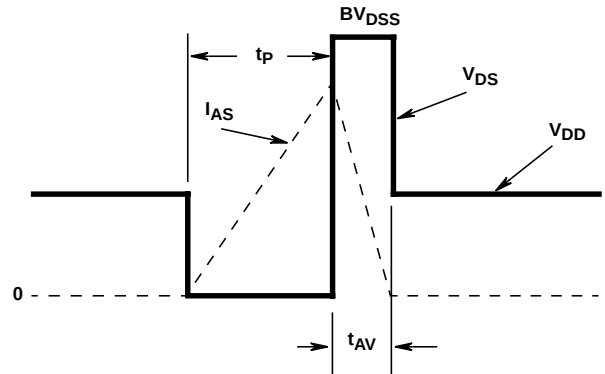


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

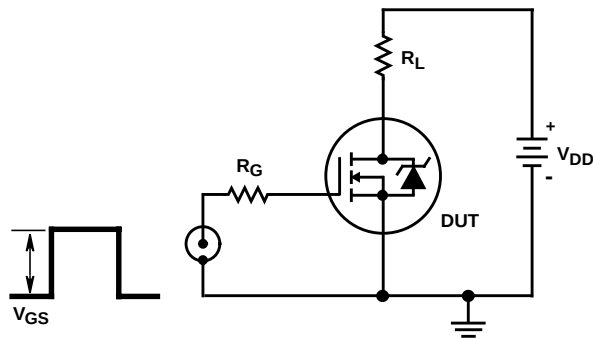


FIGURE 17. SWITCHING TIME TEST CIRCUIT

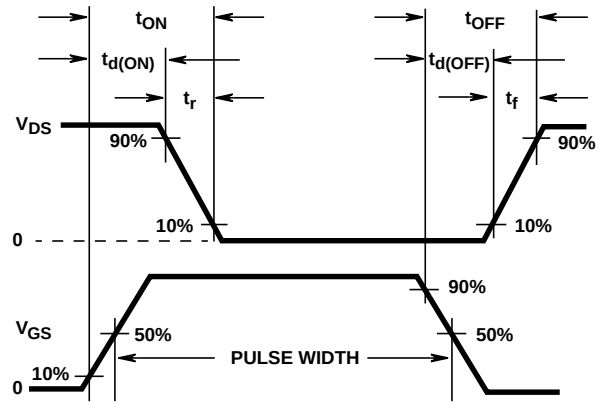


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

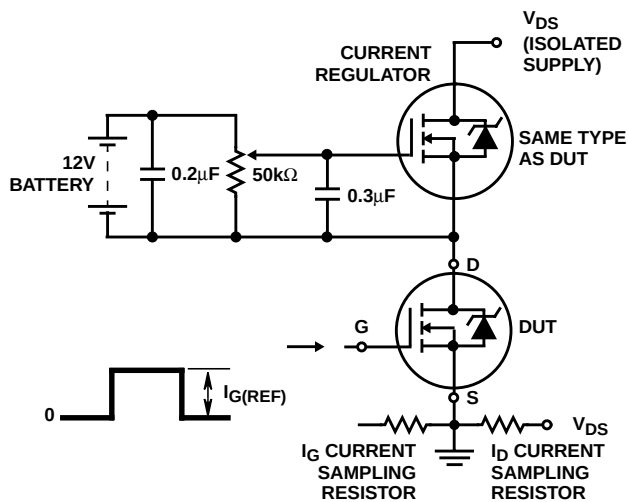


FIGURE 19. GATE CHARGE TEST CIRCUIT

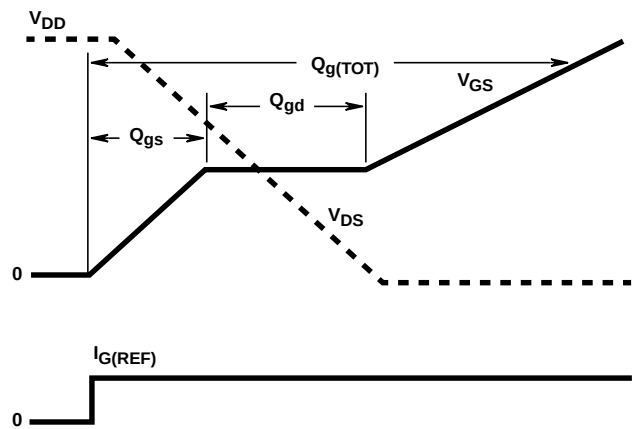


FIGURE 20. GATE CHARGE WAVEFORMS