

# HAT2043R

Silicon N Channel Power MOS FET  
High Speed Power Switching

# HITACHI

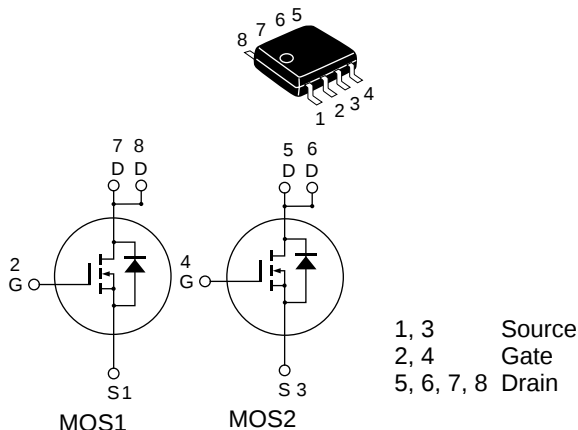
ADE-208-668D (Z)  
5th. Edition  
February 1999

## Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

## Outline

SOP-8



Absolute Maximum Ratings (Ta = 25°C)

| Item                                   | Symbol                                 | Ratings       | Unit |
|----------------------------------------|----------------------------------------|---------------|------|
| Drain to source voltage                | V <sub>DSS</sub>                       | 30            | V    |
| Gate to source voltage                 | V <sub>GSS</sub>                       | ± 20          | V    |
| Drain current                          | I <sub>D</sub>                         | 8             | A    |
| Drain peak current                     | I <sub>D(pulse)</sub> <sup>Note1</sup> | 64            | A    |
| Body-drain diode reverse drain current | I <sub>DR</sub>                        | 8             | A    |
| Channel dissipation                    | Pch <sup>Note2</sup>                   | 2.0           | W    |
| Channel dissipation                    | Pch <sup>Note3</sup>                   | 3.0           | W    |
| Channel temperature                    | Tch                                    | 150           | °C   |
| Storage temperature                    | Tstg                                   | – 55 to + 150 | °C   |

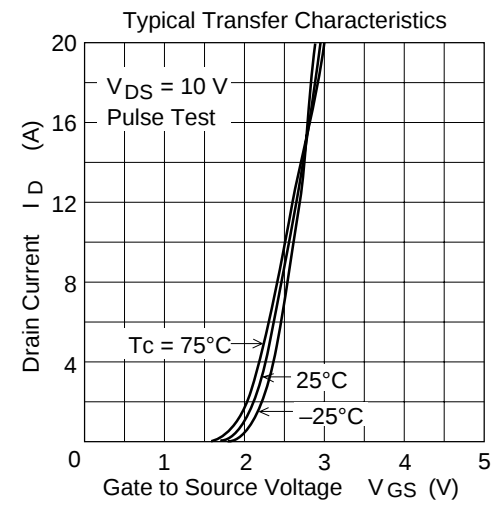
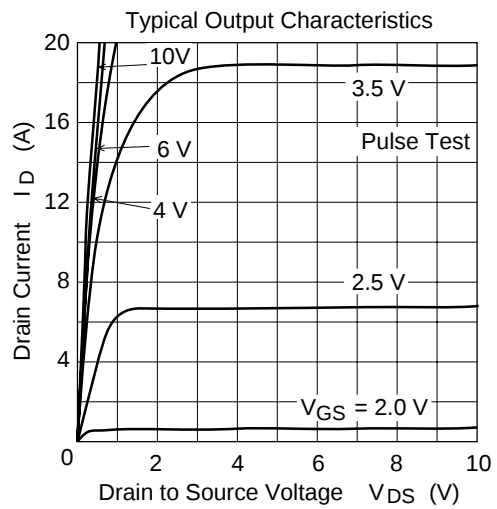
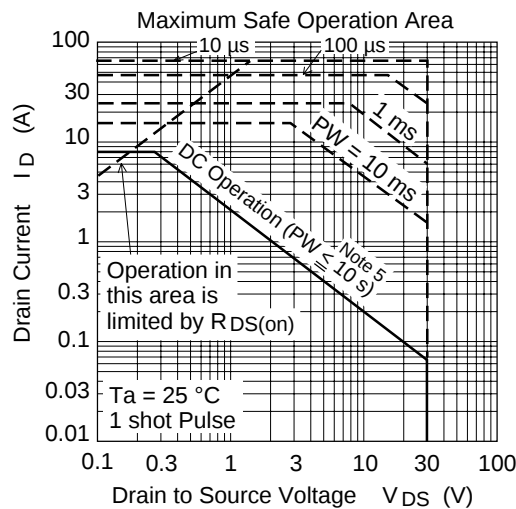
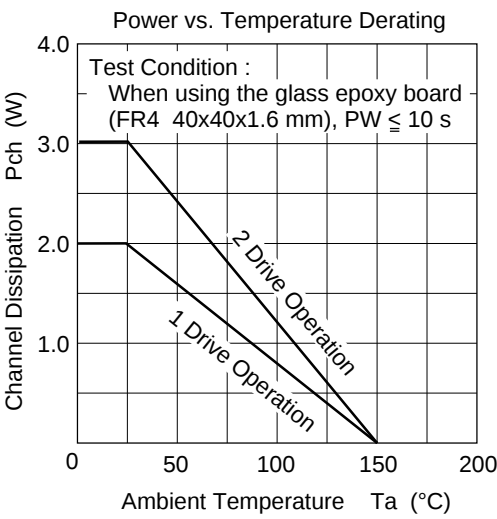
Note:    1. PW ≤ 10 μs, duty cycle ≤ 1%  
          2. 1 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s  
          3. 2 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

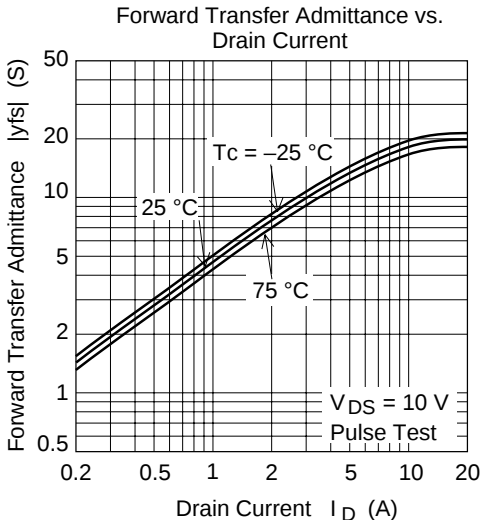
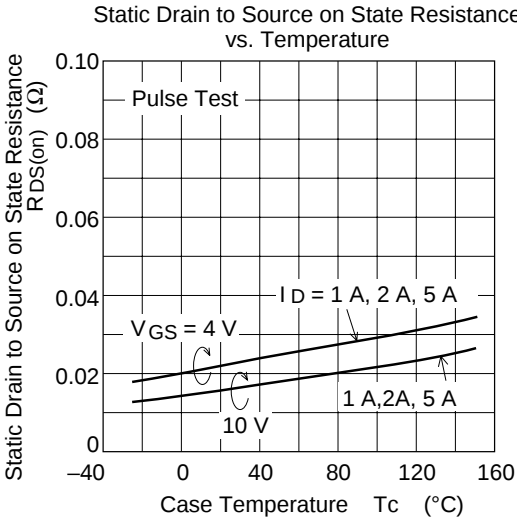
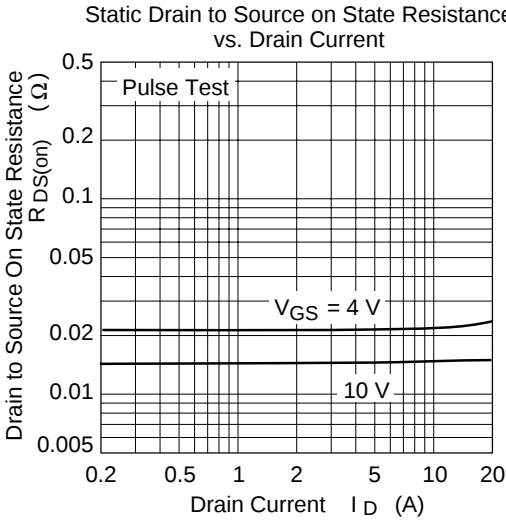
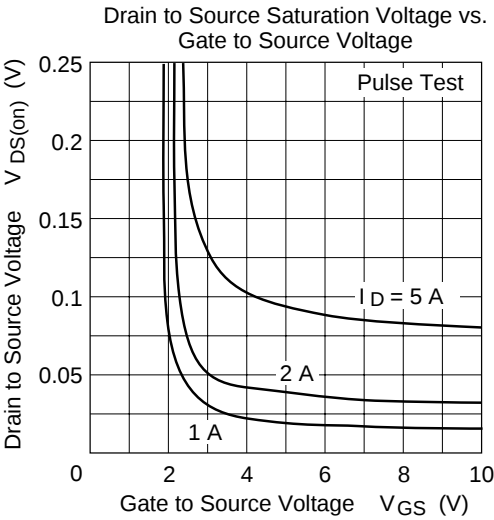
Electrical Characteristics (Ta = 25°C)

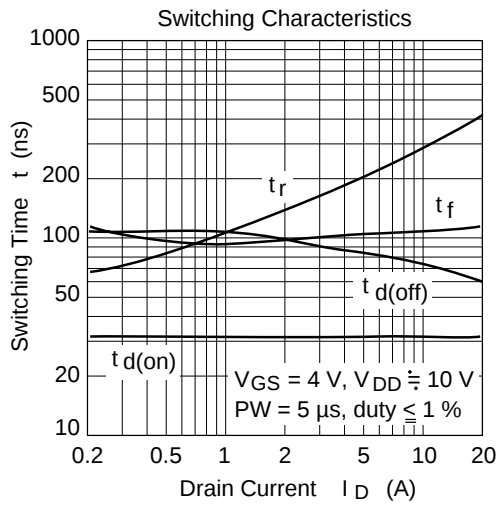
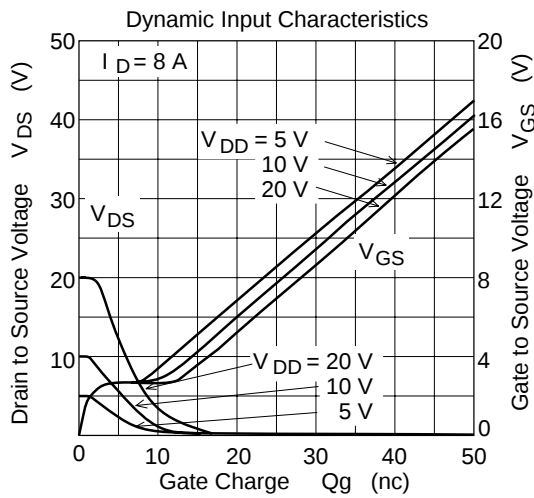
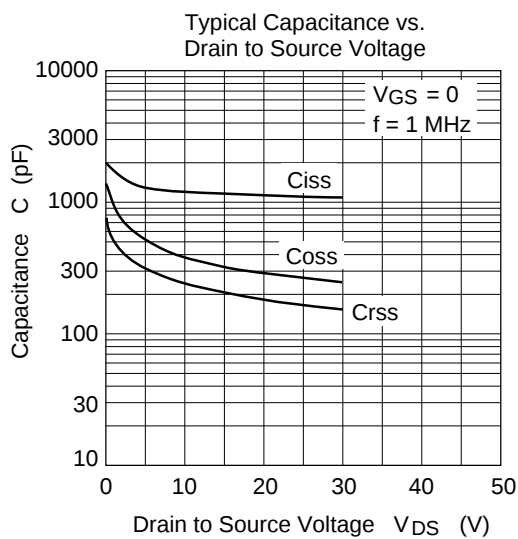
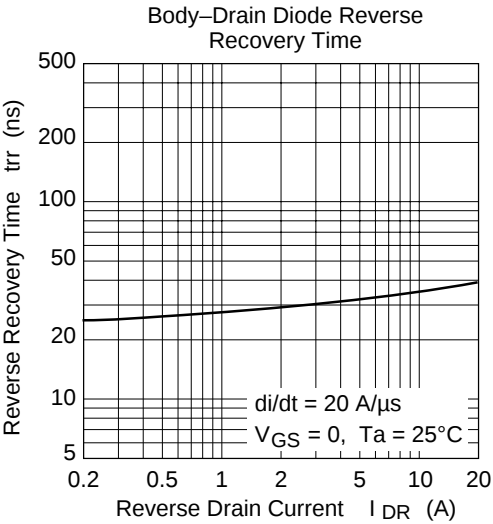
| Item                                       | Symbol               | Min | Typ   | Max   | Unit | Test Conditions                                               |
|--------------------------------------------|----------------------|-----|-------|-------|------|---------------------------------------------------------------|
| Drain to source breakdown voltage          | V <sub>(BR)DSS</sub> | 30  | —     | —     | V    | I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0                   |
| Gate to source leak current                | I <sub>GSS</sub>     | —   | —     | ± 0.1 | μA   | V <sub>GS</sub> = ± 20 V, V <sub>DS</sub> = 0                 |
| Zero gate voltege drain current            | I <sub>DSS</sub>     | —   | —     | 1     | μA   | V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0                   |
| Gate to source cutoff voltage              | V <sub>GS(off)</sub> | 1.0 | —     | 2.5   | V    | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA                 |
| Static drain to source on state resistance | R <sub>DS(on)</sub>  | —   | 0.016 | 0.022 | Ω    | I <sub>D</sub> = 4 A, V <sub>GS</sub> = 10 V <sup>Note4</sup> |
|                                            | R <sub>DS(on)</sub>  | —   | 0.022 | 0.029 | Ω    | I <sub>D</sub> = 4 A, V <sub>GS</sub> = 4 V <sup>Note4</sup>  |
| Forward transfer admittance                | y <sub>fs</sub>      | 9   | 14    | —     | S    | I <sub>D</sub> = 4 A, V <sub>DS</sub> = 10 V <sup>Note4</sup> |
| Input capacitance                          | Ciss                 | —   | 1170  | —     | pF   | V <sub>DS</sub> = 10 V                                        |
| Output capacitance                         | Coss                 | —   | 390   | —     | pF   | V <sub>GS</sub> = 0                                           |
| Reverse transfer capacitance               | Crss                 | —   | 240   | —     | pF   | f = 1 MHz                                                     |
| Total gate charge                          | Qg                   | —   | 32    | —     | nc   | V <sub>DD</sub> = 10 V                                        |
| Gate to source charge                      | Qgs                  | —   | 22    | —     | nc   | V <sub>GS</sub> = 10 V                                        |
| Gate to drain charge                       | Qgd                  | —   | 10    | —     | nc   | I <sub>D</sub> = 8 A                                          |
| Turn-on delay time                         | t <sub>d(on)</sub>   | —   | 32    | —     | ns   | V <sub>GS</sub> = 4 V, I <sub>D</sub> = 4 A                   |
| Rise time                                  | t <sub>r</sub>       | —   | 190   | —     | ns   | V <sub>DD</sub> ≅ 10 V                                        |
| Turn-off delay time                        | t <sub>d(off)</sub>  | —   | 85    | —     | ns   |                                                               |
| Fall time                                  | t <sub>f</sub>       | —   | 110   | —     | ns   |                                                               |
| Body–drain diode forward voltage           | V <sub>DF</sub>      | —   | 0.84  | 1.09  | V    | IF = 8 A, V <sub>GS</sub> = 0 <sup>Note4</sup>                |
| Body–drain diode reverse recovery time     | t <sub>rr</sub>      | —   | 35    | —     | ns   | IF = 8 A, V <sub>GS</sub> = 0<br>diF/ dt = 20 A/ μs           |

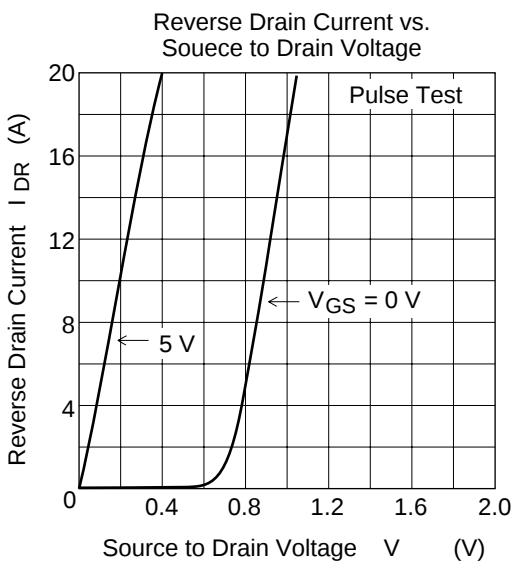
Note:    4.        Pulse test

Main Characteristics

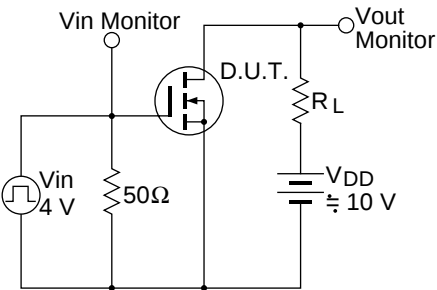




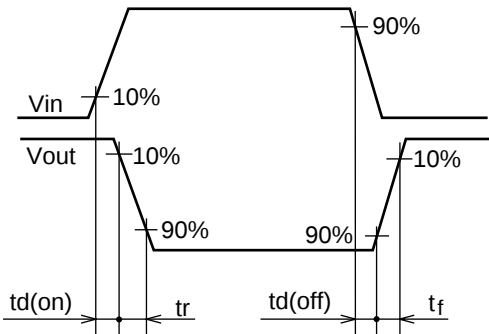




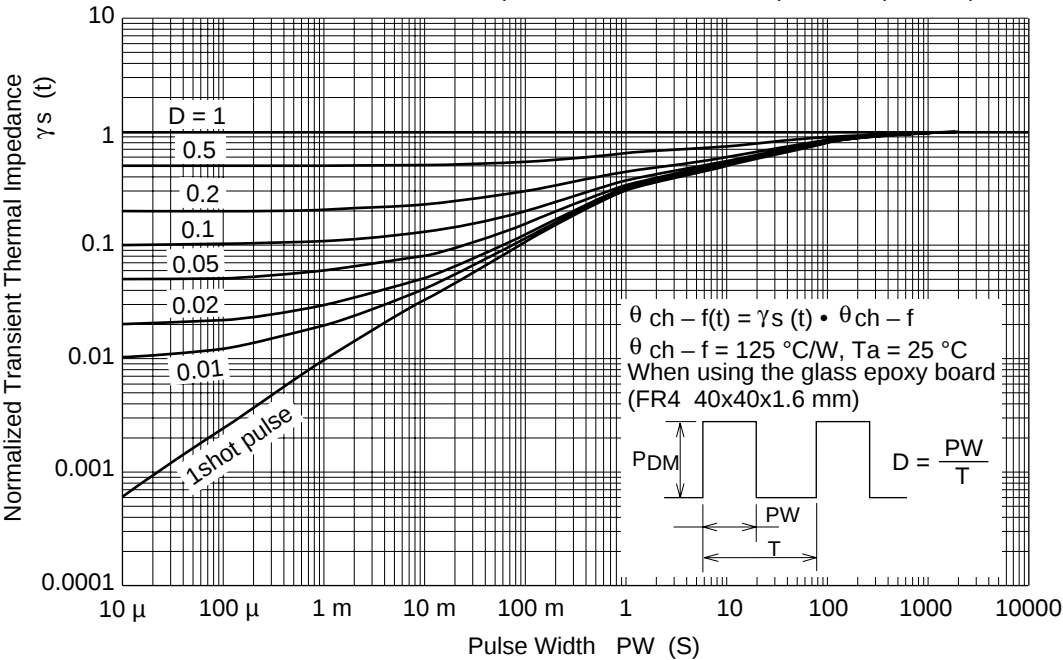
Switching Time Test Circuit



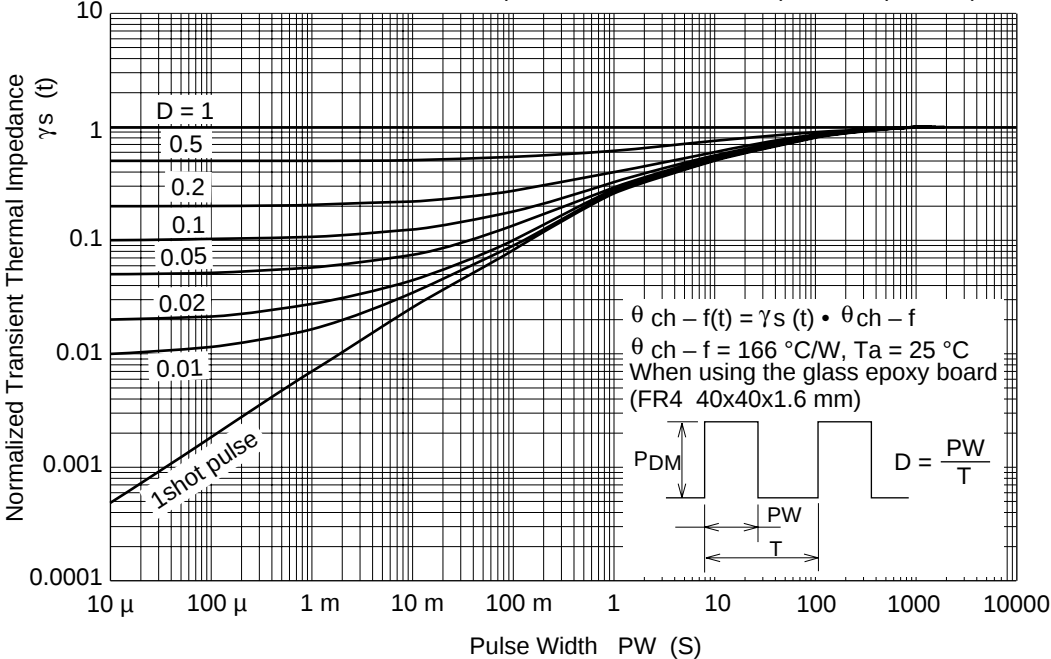
Switching Time Waveform



Normalized Transient Thermal Impedance vs. Pulse Width (1 Drive Operation)

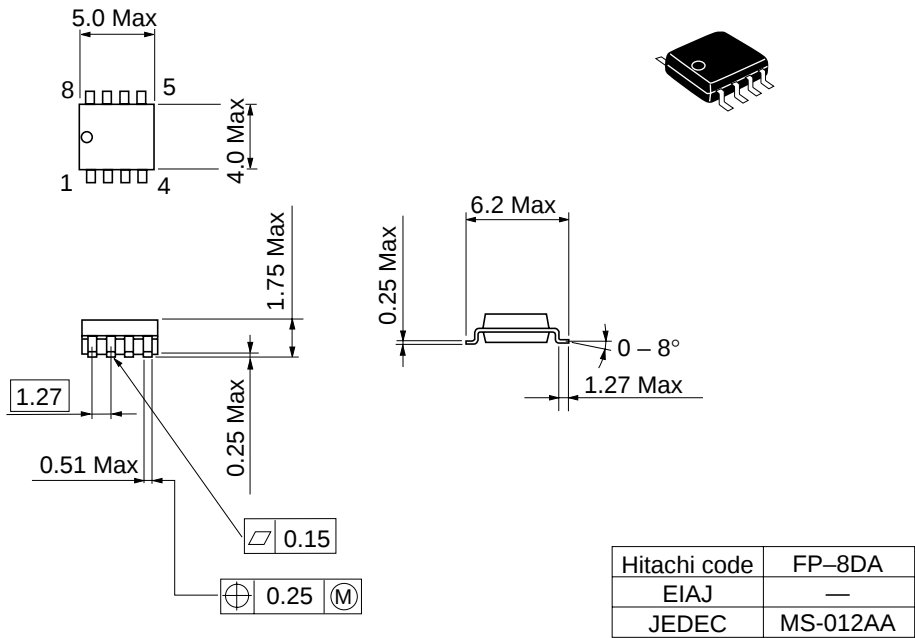


Normalized Transient Thermal Impedance vs. Pulse Width (2 Drive Operation)



Package Dimensions

Unit: mm



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