# N-Channel Power MOSFET
# (57A, 100Volts)

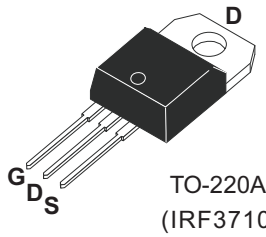
## DESCRIPTION

The Nell **IRF3710** are N-channel enhancement mode silicon gate power field effect transistors.

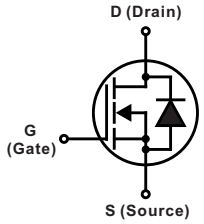
They are designed, tested and guaranteed to withstand level of energy in breakdown avalanche made of operation.

They are designed as an extremely efficient and reliable device for use in a wide variety of applications such as switching regulators, convertors, motor drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive power.

These transistors can be operated directly from integrated circuits.




TO-220AB
(IRF3710A)




## FEATURES

- $R_{DS(ON)}$ = 0.023Ω @ $V_{GS}$ = 10V
- Ultra low gate charge(130nC max.)
- Low reverse transfer capacitance ($C_{RSS}$ = 72pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 175°C operation temperature

| PRODUCT SUMMARY | |
|---|---|
| $I_D$ (A) | 57 |
| $V_{DSS}$ (V) | 100 |
| $R_{DS(ON)}$ (Ω) | 0.023 @ $V_{GS}$ = 10V |
| $Q_G$(nC) max. | 130 |

**ABSOLUTE MAXIMUM RATINGS ($T_C$ = 25°C unless otherwise specified)**

| SYMBOL | PARAMETER | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $V_{DSS}$ | Drain to Source voltage(Note 1) | $T_J$=25°C to 150°C | 100 | |
| $V_{DGR}$ | Drain to Gate voltage | $R_{GS}$=20KΩ | 100 | V |
| $V_{GS}$ | Gate to Source voltage | | ±20 | |
| $I_D$ | Continuous Drain Current | $V_{GS}$=10V, $T_C$=25°C | 57 | A |
| | | $V_{GS}$=10V, $T_C$=100°C | 40 | |
| $I_{DM}$ | Pulsed Drain current (Note 1) | | 230 | |
| $I_{AR}$ | Repetitive avalanche current (Note 1) | | 28 | |
| $E_{AR}$ | Repetitive avalanche energy(Note 1) | $I_{AR}$=28A, $R_{GS}$=50Ω, $V_{GS}$=10V | 20 | mJ |
| $E_{AS}$ | Single pulse avalanche energy (Note 2) | $I_{AS}$=28A, L=0.7mH | 280 | mJ |
| dv/dt | Peak diode recovery dv/dt(Note 3) | | 5.8 | V /ns |
| $P_D$ | Total power dissipation | $T_C$=25°C | 200 | W |
| | Derating factor above 25°C | | 1.3 | W /°C |
| $T_J$ | Operation junction temperature | | -55 to 175 | |
| $T_{STG}$ | Storage temperature | | -55 to 175 | °C |
| $T_L$ | Maximum soldering temperature, for 10 seconds | 1.6mm from case | 300 | |
| | Mounting torque, #6-32 or M3 screw | | 10 (1.1) | lbf·in (N·m) |

Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.$V_{DD}$=50V,L=0.7mH,$I_{AS}$=28A,$R_G$=25Ω, $T_J$=175°C
3.$I_{SD}$ ≤ 28A, di/dt ≤ 380A/μs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

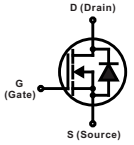
## THERMAL RESISTANCE

| SYMBOL | PARAMETER | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|
| $R_{th(j-c)}$ | Thermal resistance, junction to case | | | 0.75 | |
| $R_{th(c-s)}$ | Thermal resistance, case to heatsink | | 0.5 | | °C/W |
| $R_{th(j-a)}$ | Thermal resistance, junction to ambient | | | 62 | |

## ELECTRICAL CHARACTERISTICS ($T_C$ = 25°C unless otherwise specified)

| SYMBOL | PARAMETER | TEST CONDITIONS | | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|---|---|
| ◎ STATIC | | | | | | | |
| $V_{(BR)DSS}$ | Drain to source breakdown voltage | $V_{GS}$ = 0V, $I_D$ = 250μA | | 100 | | | V |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown voltage temperature coefficient | $I_D$ = 1mA, referenced to 25°C | | | 0.13 | | V/ºC |
| $I_{DSS}$ | Drain to source leakage current | $V_{DS}$=100V, $V_{GS}$=0V | $T_C$ = 25°C | | | 25 | μA |
| | | $V_{DS}$=80V, $V_{GS}$=0V | $T_C$=150°C | | | 250 | |
| $I_{GSS}$ | Gate to source forward leakage current | $V_{GS}$ = 20V, $V_{DS}$ = 0V | | | | 100 | nA |
| | Gate to source reverse leakage current | $V_{GS}$ = -20V, $V_{DS}$ = 0V | | | | -100 | |
| $R_{DS(ON)}$ | Static drain to source on-state resistance | $V_{GS}$ = 10V, $I_D$ = 28A (Note 1) | | | | 0.023 | Ω |
| $V_{GS(TH)}$ | Gate threshold voltage | $V_{GS}$=$V_{DS}$, $I_D$=250μA | | 2 | | 4 | V |
| $g_{fs}$ | Forward transconductance | $V_{DS}$=25V, $I_D$=28A | | 32 | | | S |
| ◎ DYNAMIC | | | | | | | |
| $C_{ISS}$ | Input capacitance | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f =1MHz | | | 3130 | | pF |
| $C_{OSS}$ | Output capacitance | | | | 410 | | |
| $C_{RSS}$ | Reverse transfer capacitance | | | | 72 | | |
| $t_{d(ON)}$ | Turn-on delay time | $V_{DD}$ = 50V, $I_D$ = 28A<br>$V_{GS}$ = 10V, $R_G$=2.5Ω (Note 1) | | | 12 | | ns |
| $t_r$ | Rise time | | | | 58 | | |
| $t_{d(OFF)}$ | Turn-off delay time | | | | 45 | | |
| $t_f$ | Fall time | | | | 47 | | |
| $L_D$ | Internal drain inductance | Between lead, 6mm from package and center of die | | | 4.5 | | nH |
| $L_S$ | Internal source inductance | | | | 7.5 | | |
| $Q_G$ | Total gate charge | $V_{DS}$ = 80V, $V_{GS}$ = 10V, $I_D$ = 28A | | | | 130 | nC |
| $Q_{GS}$ | Gate to source charge | | | | | 26 | |
| $Q_{GD}$ | Gate to drain charge (Miller charge) | | | | | 43 | |

## SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C$ = 25°C unless otherwise specified)

| SYMBOL | PARAMETER | TEST CONDITIONS | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|---|
| $V_{SD}$ | Diode forward voltage | $I_{SD}$ = 28A, $V_{GS}$ = 0V | | | 1.2 | V |
| $I_S(I_{SD})$ | Continuous source to drain current | Integral reverse P-N junction diode in the MOSFET | | | 57 | A |
| $I_{SM}$ | Pulsed source current |  | | | 230 | |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 28A, $V_{GS}$ = 0V, $dI_F/dt$ = 100A/μs | | 140 | 220 | ns |
| $Q_{rr}$ | Reverse recovery charge | | | 670 | 1010 | nC |
| $t_{ON}$ | Forward turn-on time | Intrinsic turn-on time is negligible (turn-on is domonated by LS+LD) | | | | |

Note: 1. Pulse test: Pulse width ≤ 400μs, duty cycle ≤ 2%.

## ORDERING INFORMATION SCHEME

**IRF 3710 A**

**MOSFET series**

N-Channel, IR series

**Current & Voltage rating, $I_D$ & $V_{DS}$**

57A / 100V

**Package type**

A = TO-220AB

**Fig.1 Typical output characteristics, $T_C$=25°C**

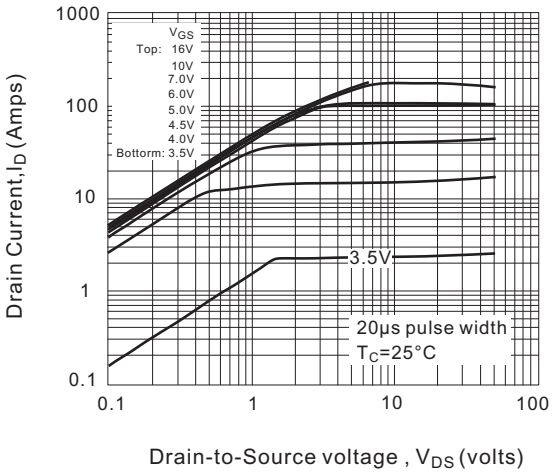



**Fig.2 Typical output characteristics, $T_C$=150°C**

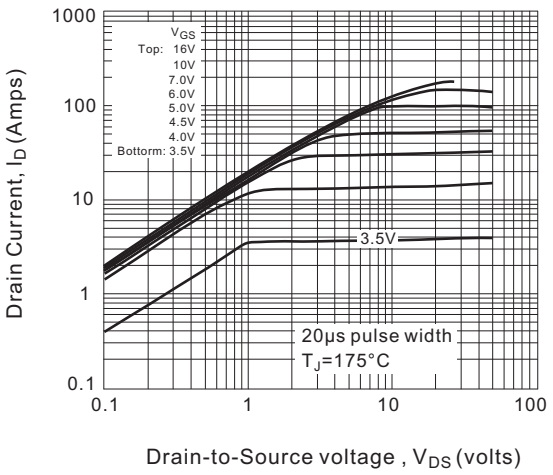



**Fig.3 Typical transfer characteristics**

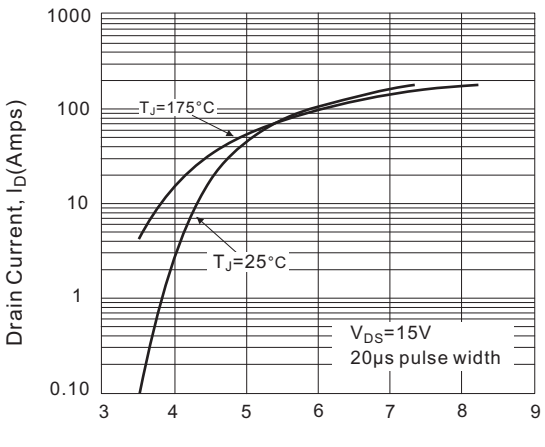



**Fig.4 Normalized On-Resistance vs. Temperature**

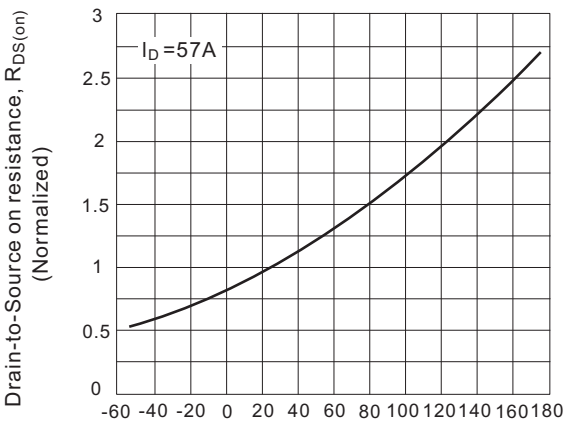


**Fig.5 Typical capacitance vs. Drain-to-Source voltage**

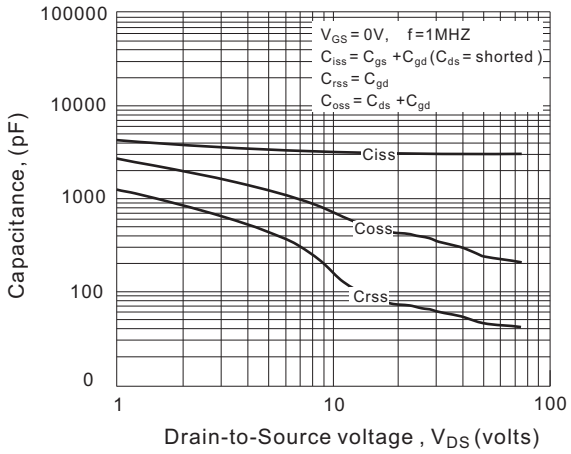



**Fig.6 Typical source-drain diode forward voltage**

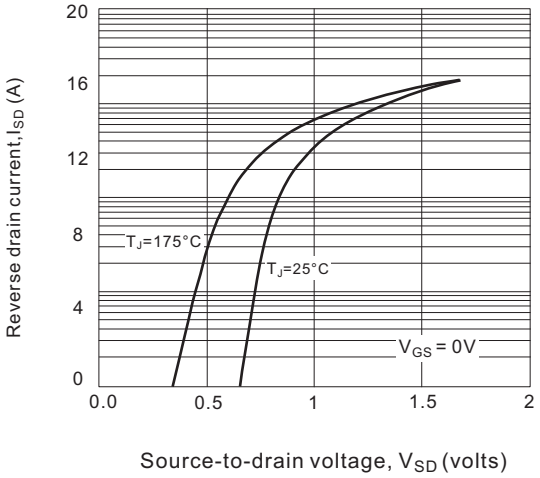



**Fig.7 Typical gate charge vs. gate-to-source voltage**

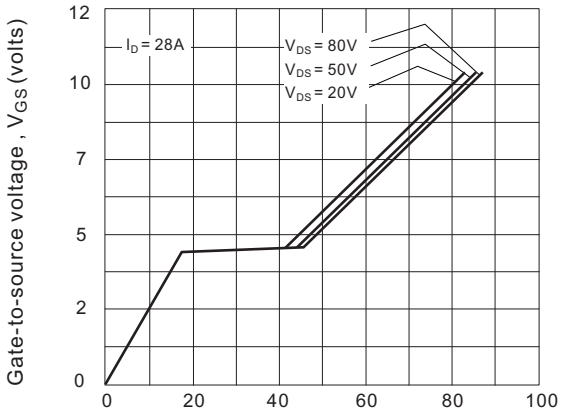



**Fig.8 Maximum safe operating area**

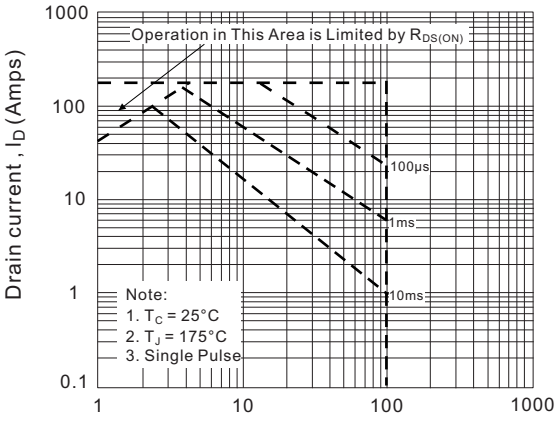



**Fig.9 Maximum drain current vs. Case temperature**

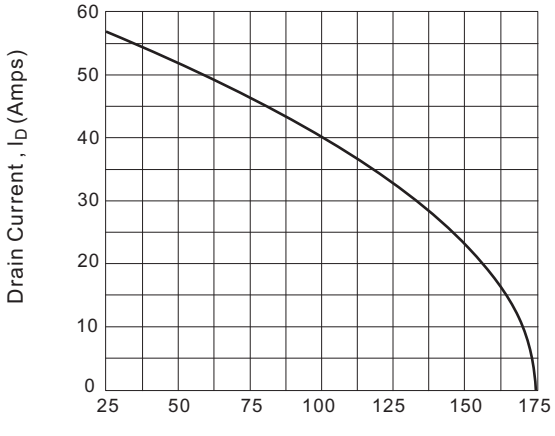


**Fig.10 Maximum effective transient thermal impedance, Junction-to-Case**

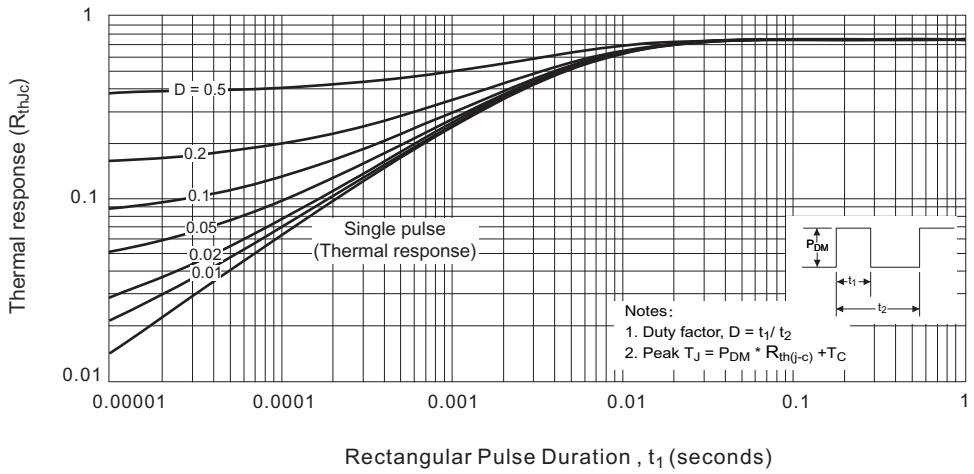



**Fig.11a. Switching time test circuit**

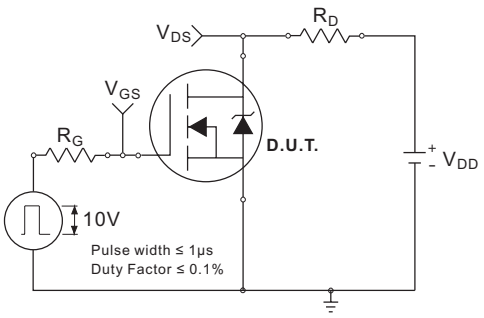



**Fig.11b. Switching time waveforms**

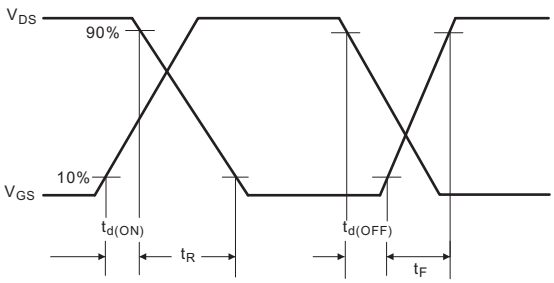



**Fig.12a. Unclamped Inductive test circuit**

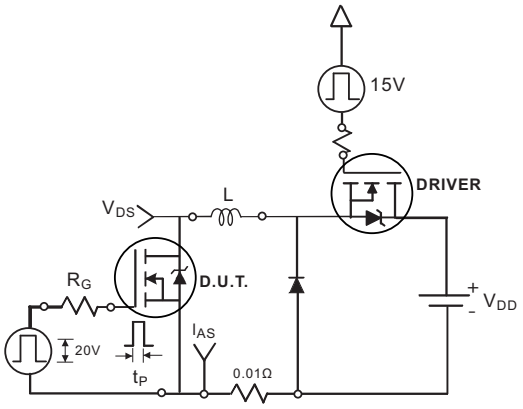
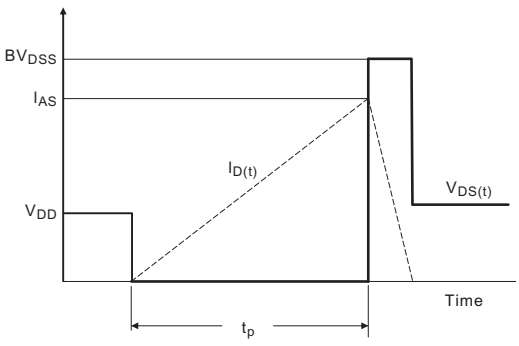



**Fig.12b. Unclamped Inductive waveforms**




Vary $t_p$ to obtain required $I_{AS}$

**Fig.12c. Maximum avalanche energy vs. Drain current**

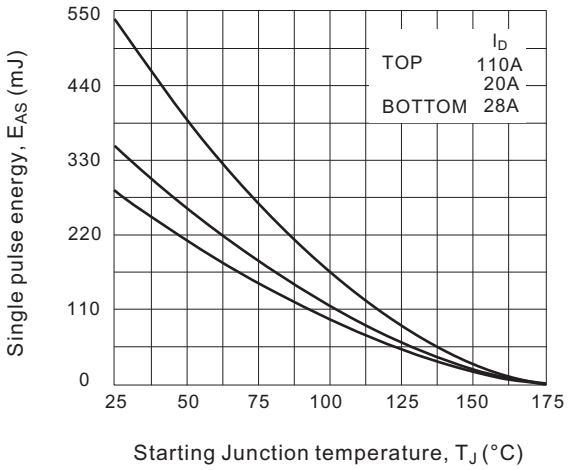



**Fig.13a. Basic gate charge waveform**

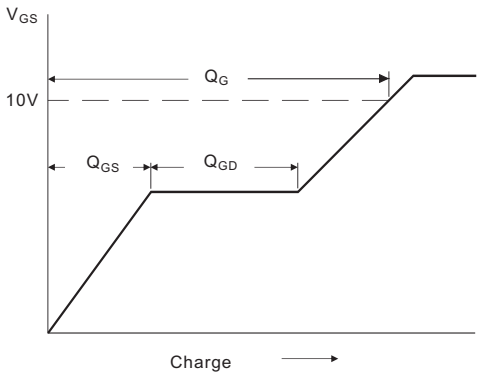



**Fig.13b. Gate charge test circuit**

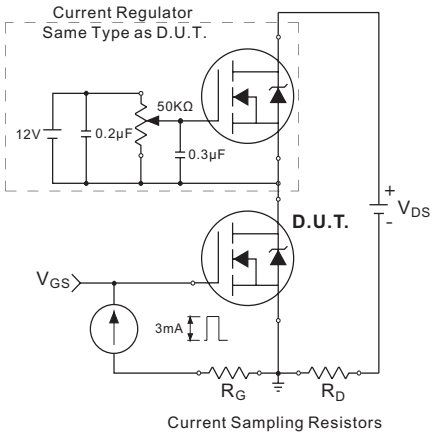
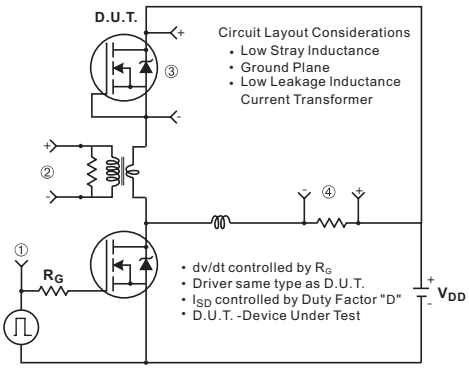
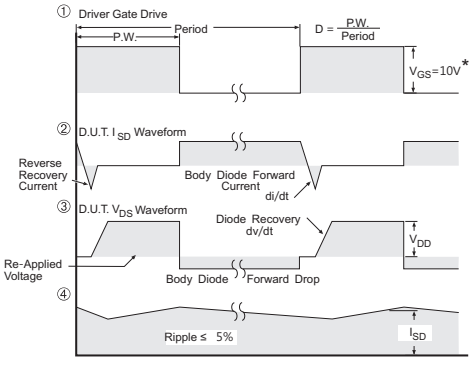



**Fig.14 Peak diode recovery dv/dt test circuit for N-Channel MOSFET**

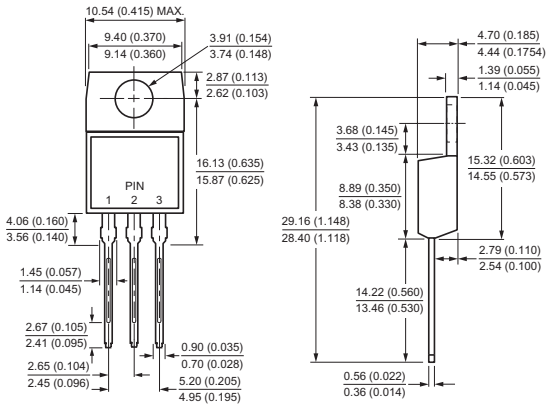


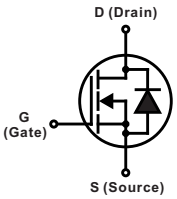




*$V_{GS}$ = 5V for Logic Level Devices and 3V for drive devices

## Case Style

**TO-220AB**




All dimensions in millimeters(inches)