

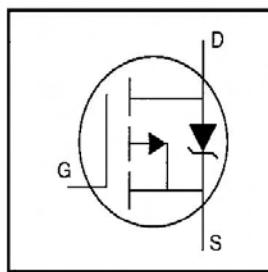
# International **IR** Rectifier

PD-95976

## IRFI9Z24GPbF

### HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- P-Channel
- 175°C Operating Temperature
- Dynamic dv/dt Rating
- Low Thermal Resistance
- Lead-Free

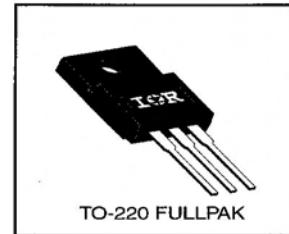


$V_{DSS} = -60V$   
 $R_{DS(on)} = 0.28\Omega$   
 $I_D = -8.5A$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-8.5	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-6.0	
$I_{DM}$	Pulsed Drain Current ①	-34	
$P_D @ T_C = 25^\circ C$	Power Dissipation	37	W
	Linear Derating Factor	0.24	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	200	mJ
$I_{AR}$	Avalanche Current ①	-8.5	A
$E_{AR}$	Repetitive Avalanche Energy ①	3.7	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	-4.5	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{JC}$	Junction-to-Case	—	—	4.1	°C/W
$R_{JA}$	Junction-to-Ambient	—	—	65	

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Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-60	—	—	V	$V_{GS}=0\text{V}$ , $I_D=-250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.056	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.28	$\Omega$	$V_{GS}=-10\text{V}$ , $I_D=-5.1\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$
$g_{fs}$	Forward Transconductance	3.2	—	—	S	$V_{DS}=-25\text{V}$ , $I_D=-5.1\text{A}$ ④
$I_{DS(on)}$	Drain-to-Source Leakage Current	—	—	-100	$\mu\text{A}$	$V_{DS}=-60\text{V}$ , $V_{GS}=0\text{V}$
		—	—	-500		$V_{DS}=-48\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS}=-20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS}=20\text{V}$
$Q_g$	Total Gate Charge	—	—	19	nC	$I_D=-11\text{A}$
$Q_{gs}$	Gate-to-Source Charge	—	—	5.4		$V_{DS}=-48\text{V}$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	11		$V_{GS}=-10\text{V}$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	13	—		$V_{DD}=-30\text{V}$
$t_r$	Rise Time	—	68	—		$I_D=-11\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	15	—		$R_G=18\Omega$
$t_f$	Fall Time	—	29	—		$R_D=2.5\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	570	—	pF	$V_{GS}=0\text{V}$
$C_{oss}$	Output Capacitance	—	360	—		$V_{DS}=-25\text{V}$
$C_{rss}$	Reverse Transfer Capacitance	—	65	—		$f=1.0\text{MHz}$ See Figure 5
$C$	Drain to Sink Capacitance	—	12	—	pF	$f=1.0\text{MHz}$

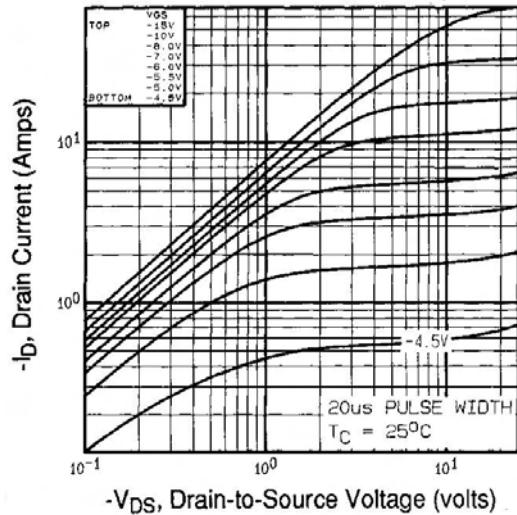
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-8.5		MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-34	A	
$V_{SD}$	Diode Forward Voltage	—	—	-6.3	V	$T_J=25^\circ\text{C}$ , $I_S=-8.5\text{A}$ , $V_{GS}=0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	100	200	ns	$T_J=25^\circ\text{C}$ , $I_F=-11\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	0.32	0.64	$\mu\text{C}$	$di/dt=100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

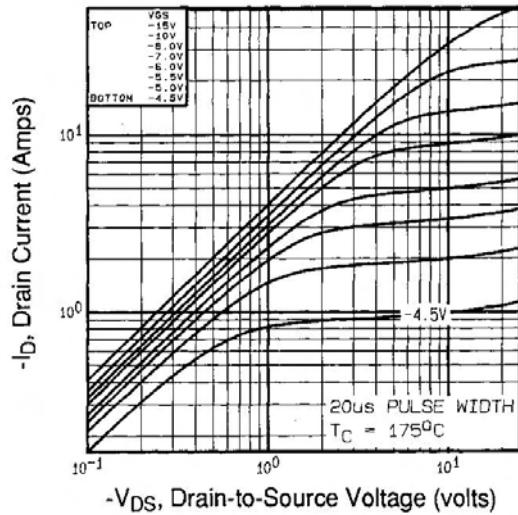
## Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11) ③  $I_{SD} \leq 11\text{A}$ ,  $di/dt \leq 140\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$  ⑤  $t=60\text{s}$ ,  $f=60\text{Hz}$

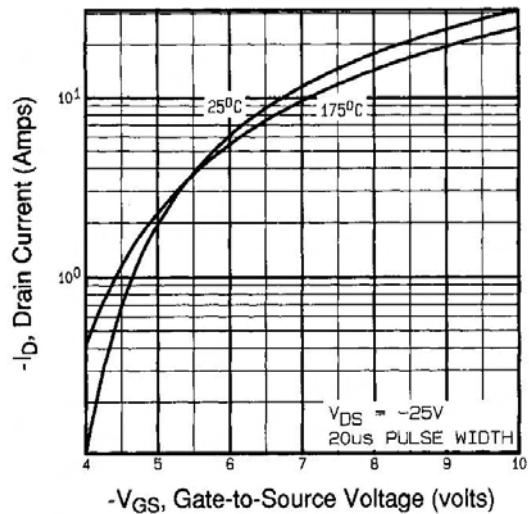
②  $V_{DD}=-25\text{V}$ , starting  $T_J=25^\circ\text{C}$ ,  $L=3.2\text{mH}$   $R_G=25\Omega$ ,  $I_{AS}=-8.5\text{A}$  (See Figure 12) ④ Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .



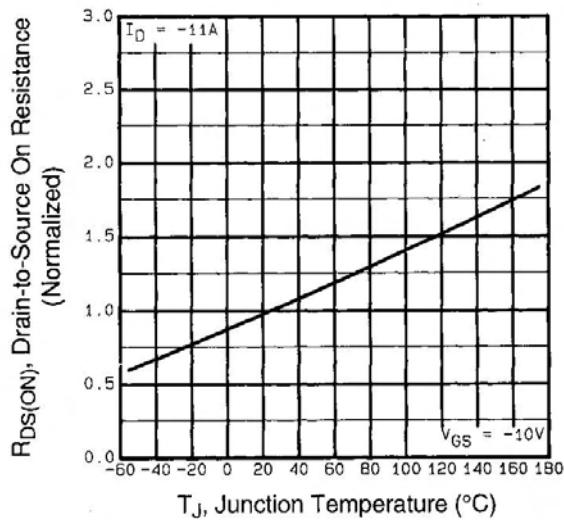
**Fig 1.** Typical Output Characteristics,  
 $T_C=25^\circ\text{C}$



**Fig 2.** Typical Output Characteristics,  
 $T_C=175^\circ\text{C}$



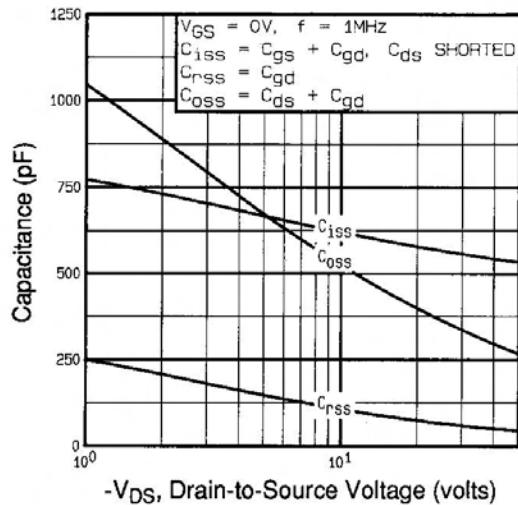
**Fig 3.** Typical Transfer Characteristics



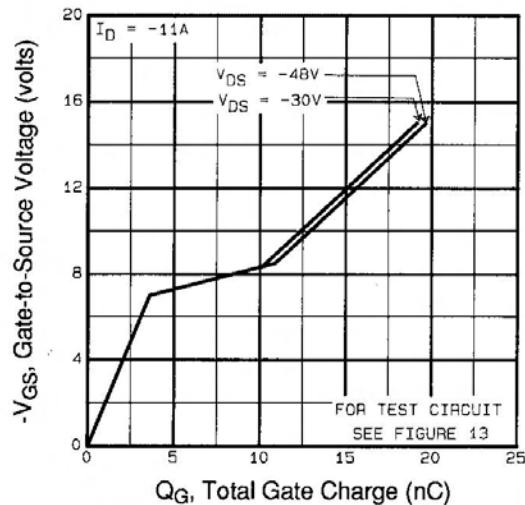
**Fig 4.** Normalized On-Resistance  
Vs. Temperature

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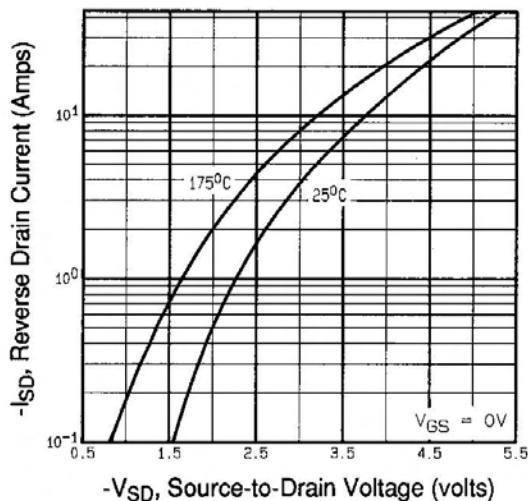
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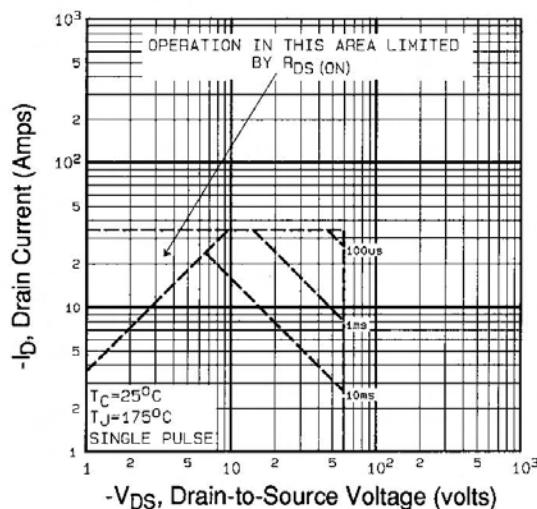
**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



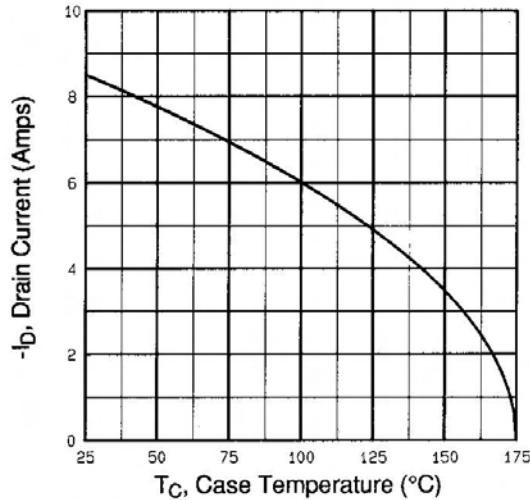
**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage



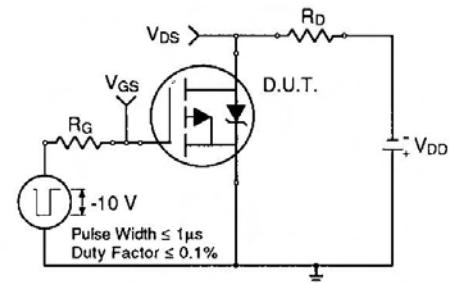
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



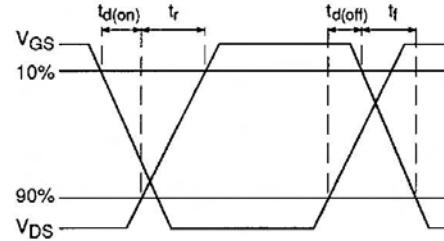
**Fig 8.** Maximum Safe Operating Area



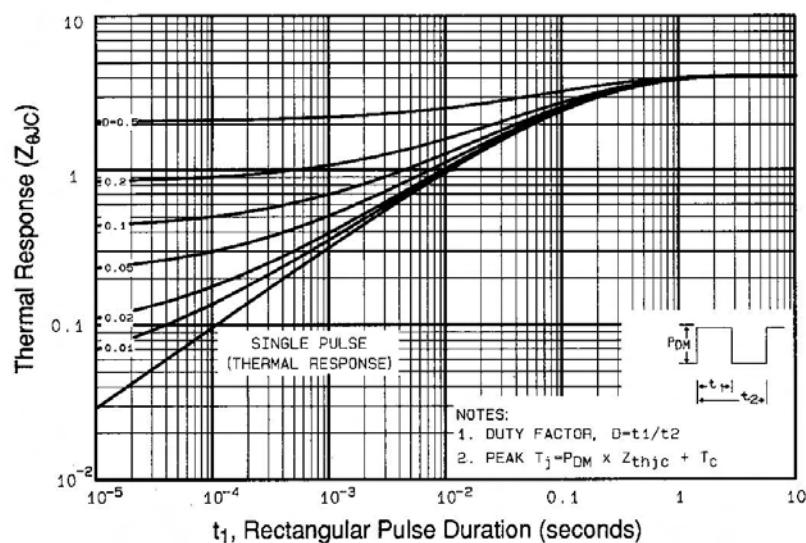
**Fig 9.** Maximum Drain Current Vs.  
Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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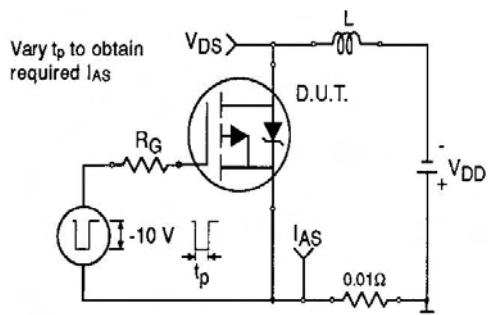


Fig 12a. Unclamped Inductive Test Circuit

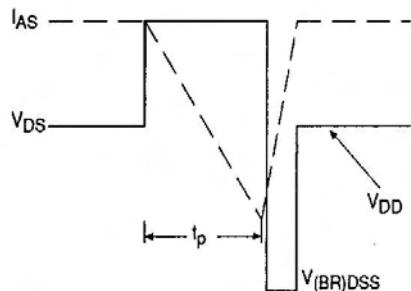


Fig 12b. Unclamped Inductive Waveforms

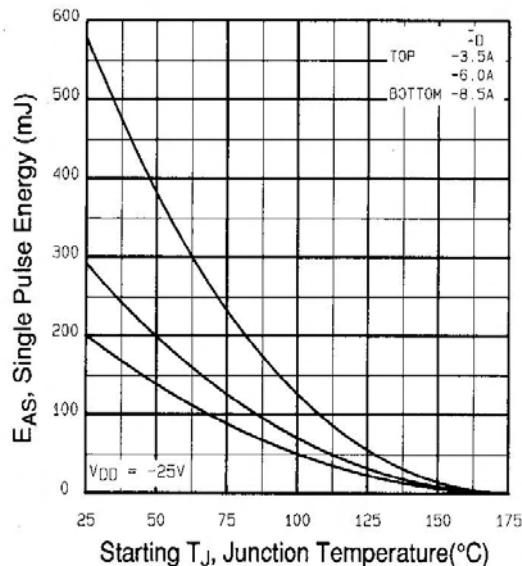


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

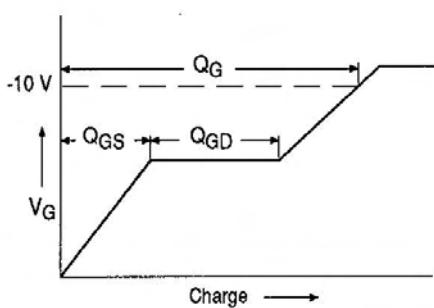


Fig 13a. Basic Gate Charge Waveform

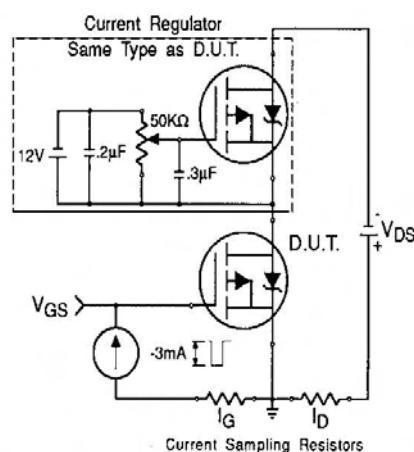
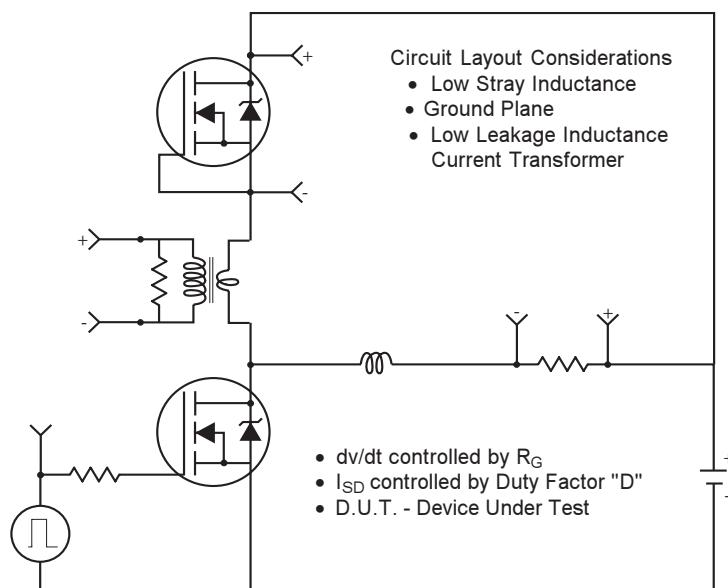


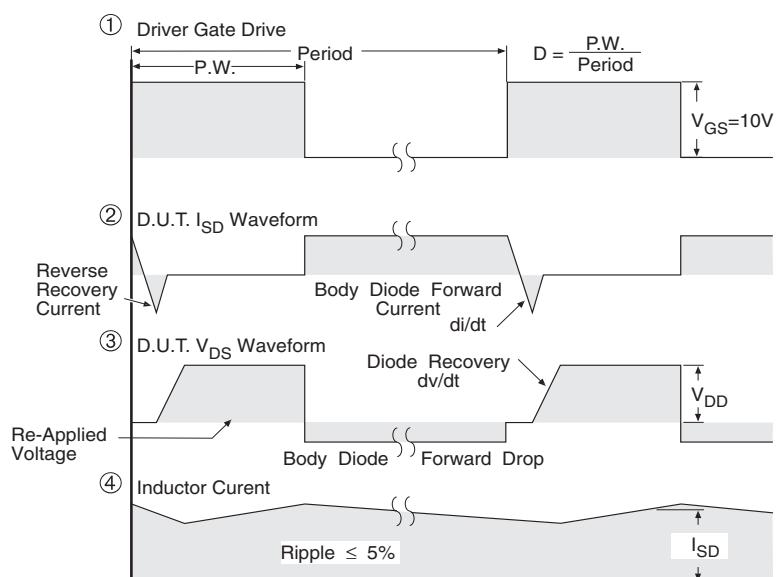
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery  $dv/dt$  Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



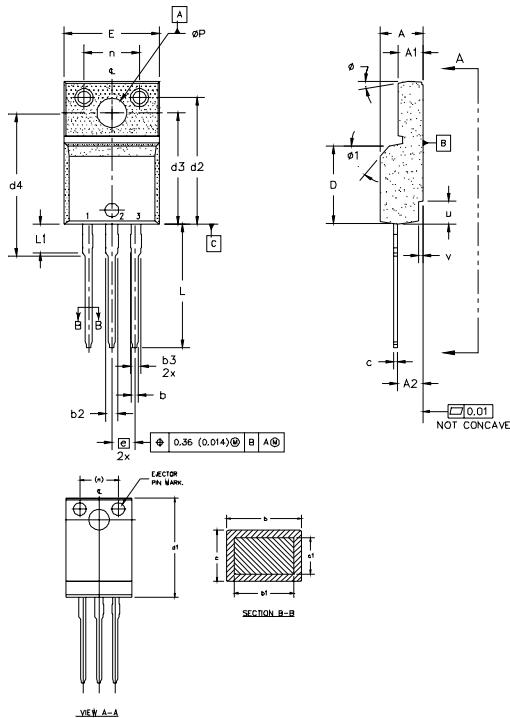
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

Fig 14 For P Channel HEXFETs

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## TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



NOTES:  
 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.  
 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].  
 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.  
 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.  
 5.0 DIMENSION b1 APPLY TO BASE METAL ONLY.  
 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.  
 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS		NOTES	
	MILLIMETERS	INCHES		
	MIN.	MAX.		
A	4.57	4.83	0.180	0.190
A1	2.57	2.83	0.101	0.114
A2	2.51	2.85	0.099	0.112
b	0.622	0.89	0.024	0.035
b1	0.622	0.838	0.024	0.033
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
c1	0.440	0.584	0.017	0.023
D	8.65	9.80	0.341	0.386
d1	15.80	16.12	0.622	0.635
d2	13.97	14.22	0.550	0.560
d3	12.30	12.92	0.484	0.509
d4	8.64	9.91	0.340	0.390
E	10.36	10.63	0.408	0.419
e	2.54 BSC	0.100 BSC		
L	15.20	13.73	0.520	0.541
L1	3.10	3.50	0.122	0.138
n	6.05	6.15	0.238	0.242
øP	3.05	3.45	0.120	0.136
u	2.40	2.50	0.094	0.098
v	0.40	0.50	0.016	0.020
ø	3"	7"	7"	7"
ø1		45°		45°

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### LEAD ASSIGNMENTS

#### HEXFET

1. GATE
2. DRAIN
3. SOURCE

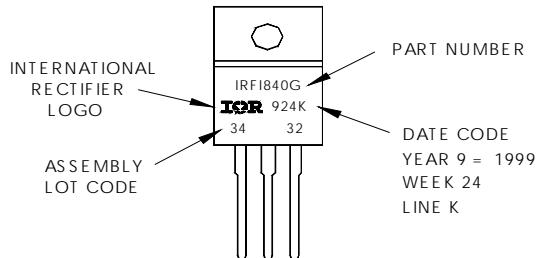
#### IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. Emitter

## TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G  
WITH ASSEMBLY  
LOT CODE 3432  
ASSEMBLED ON WW 24 1999  
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line  
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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12/04



### Notice

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