International Rectifier

SMPS MOSFET

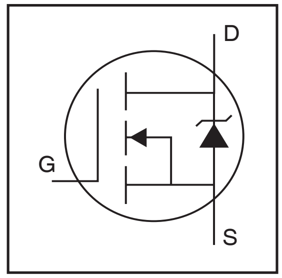
IRFP22N60C3PbF

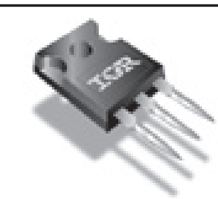
Superjunction Power MOSFET

Applications
- PFC and Primary Switch in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits
- Lead-Free

V_{DSS}@T_J max	$R_{DS(on)}$ typ.	I_D
650V	155mΩ	22A①

Benefits
- Ultra Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current





TO-247AC

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	22①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	13①	
I_{DM}	Pulsed Drain Current ②	50	
P_D @T_C = 25°C	Maximum Power Dissipation	280	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
V_{GS}	Gate-to-Source Voltage (Repetitive Peak)	± 30⑦	
dv/dt	Peak Diode Recovery dv/dt ④	9.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
I_{AR}	Avalanche Current ②	—	10	A
E_{AS} (tested)	Single Pulse Avalanche Energy ③	—	690	mJ
E_{AR}	Repetitive Avalanche Energy	See Figure 14		

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	—	0.50	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

2/11/04

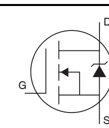
Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	——	——	V	V_{GS} = 0V, I_D = 250μA
$V_{(BR)DS}$	Drain-to-Source Avalanche Breakdown Voltage	——	770	——		V_{GS} = 0V, I_D = 10mA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.75	——	V/°C	Reference to 25°C, I_D = 1mA②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	155	190	mΩ	V_{GS} = 10V, I_D = 14A⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} = 600V, V_{GS} = 0V ⑨
		——	——	100		V_{DS} = 600V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	15	——	——	S	V_{DS} = 50V, I_D = 13A
Q_g	Total Gate Charge	——	85	130	nC	I_D = 22A
Q_{gs}	Gate-to-Source Charge	——	17	——		V_{DS} = 480V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	29	——		V_{GS} = 10V ⑤
R_G	Gate Input Resistance	——	0.8	——	Ω	f = 1MHz, open drain
$t_{d(on)}$	Turn-On Delay Time	——	14	——	ns	V_{DD} = 380V
t_r	Rise Time	——	39	——		I_D = 22A
$t_{d(off)}$	Turn-Off Delay Time	——	93	——		R_G = 9.1Ω
t_f	Fall Time	——	60	——		V_{GS} = 13V ⑤
C_{iss}	Input Capacitance	——	2910	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	190	——		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	——	25	——		f = 1.0MHz
Coss eff. (ER)	Effective Output Capacitance (Energy Related)⑧	——	94	——		V_{GS} = 0V, V_{DS} = 0V to 480V ⑧, See Fig.10
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑥	——	170	——		V_{GS} = 0V, V_{DS} = 0V to 480V ⑥, See Fig. 7

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	22①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②⑦	——	——	50	A	
V_{SD}	Diode Forward Voltage	——	——	1.2	V	T_J = 25°C, I_S = 22A, V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	——	440	660	ns	T_J = 25°C, I_F = I_S
Q_{rr}	Reverse Recovery Charge	——	7.7	1.2	μC	di/dt = 100A/μs ⑤
I_{RRM}	Reverse Recovery Current	——	33	——	A	V_R = 25V
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Limited by maximum temperature.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Starting T_J = 25°C, L=13.8mH, R_G = 25Ω, I_{AS} = 10A, V_{DD} = 50V. Eas is limited by T_J max to 210mJ. (See figure 14.)

④ $I_{SD} \le$ 22A, di/dt $\le$ 470A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 150°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ Assumes Vgs = 30V for a maximum lifetime duration of 2 hrs. or less.

⑧ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑨ 25μA max. at the end of stress tests.

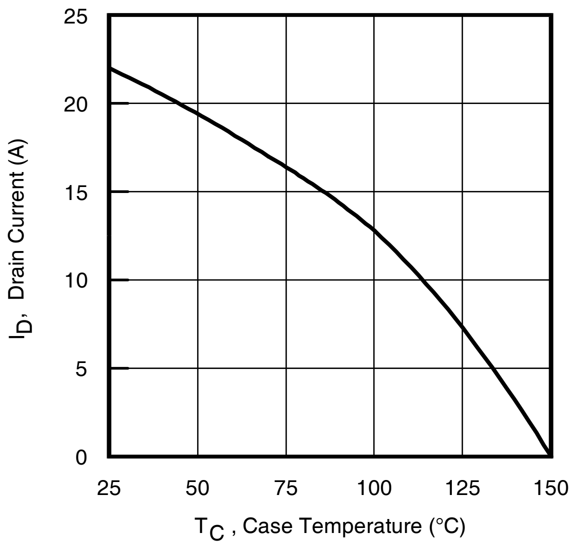


Fig 1. Maximum Drain Current vs. Case Temperature

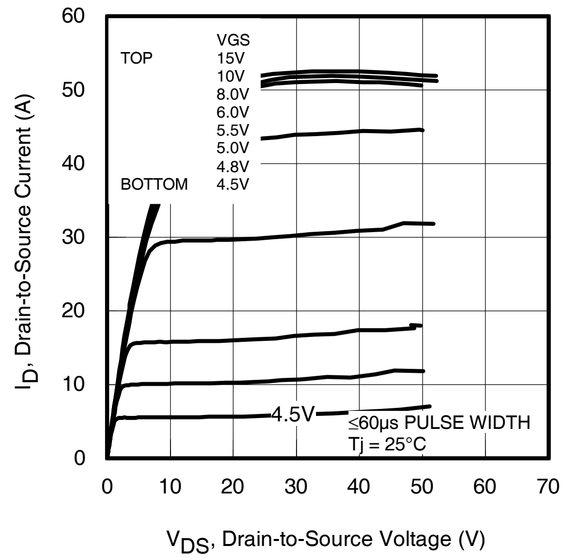


Fig 2. Typical Output Characteristics

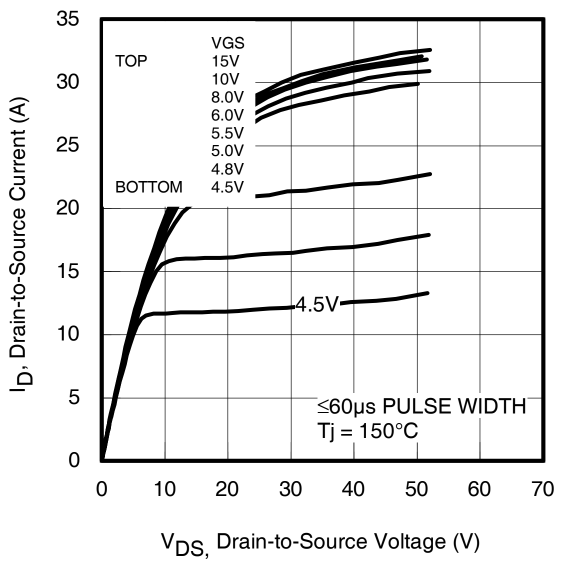


Fig 3. Typical Output Characteristics

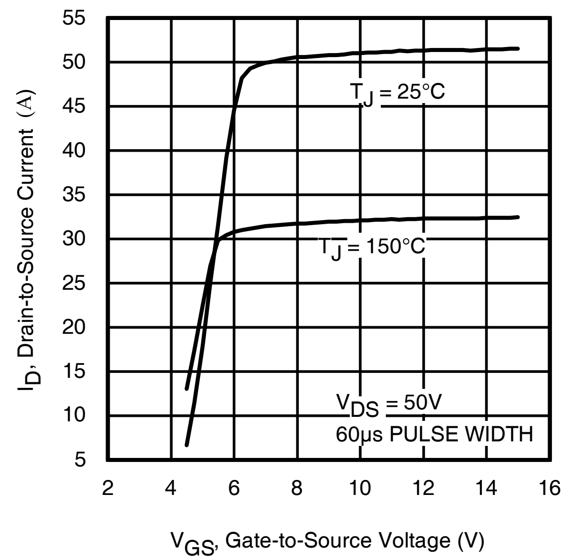


Fig 4. Typical Transfer Characteristics

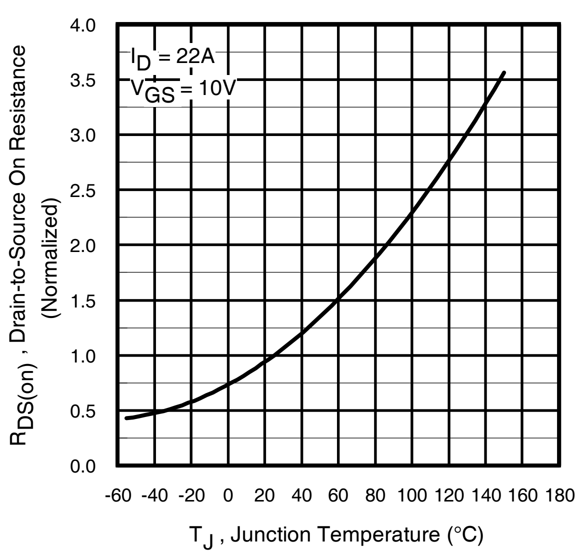


Fig 5. Normalized On-Resistance vs. Temperature

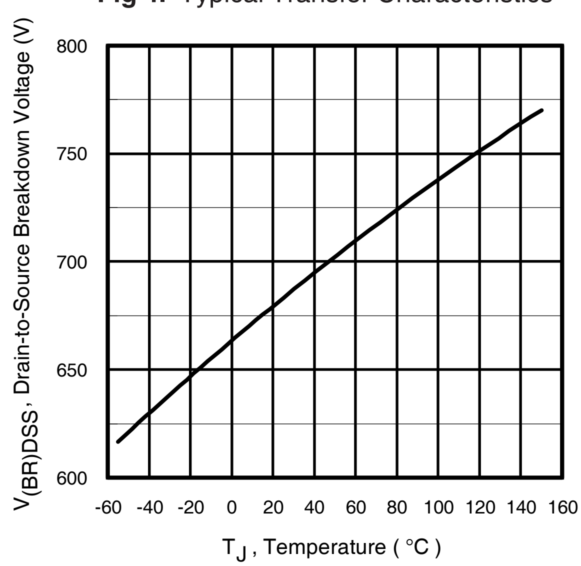


Fig 6. Drain-to-Source Breakdown Voltage

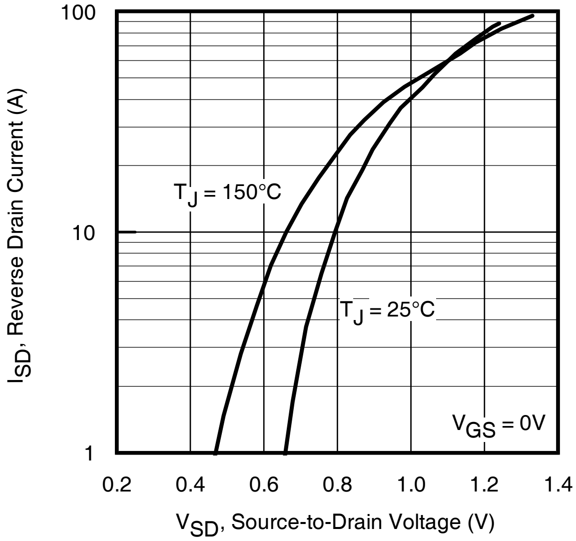


Fig 7. Typical Source-Drain Diode Forward Voltage

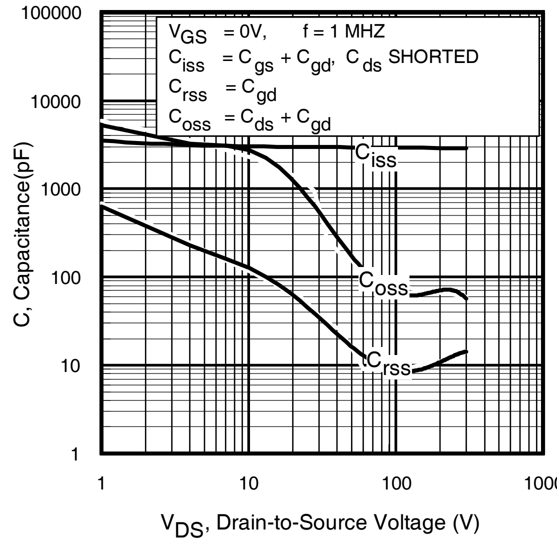


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

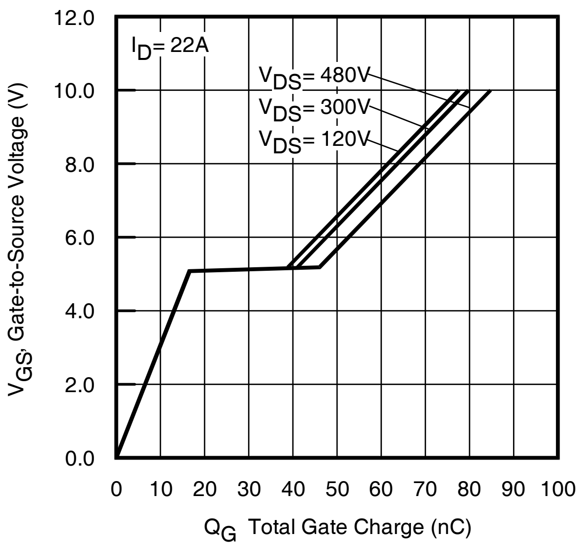


Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

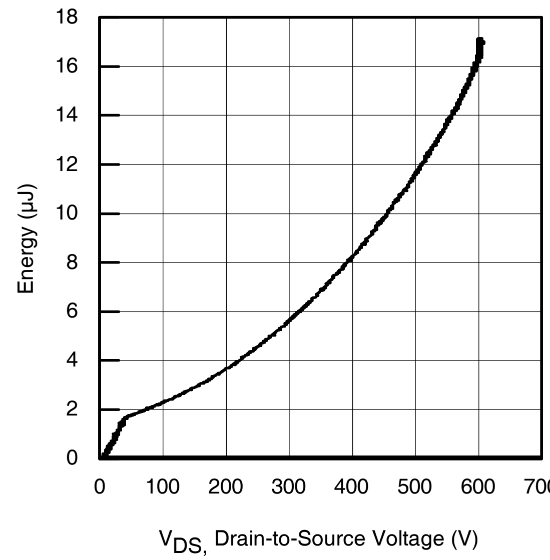


Fig 10. Typical C_{OSS} Stored Energy

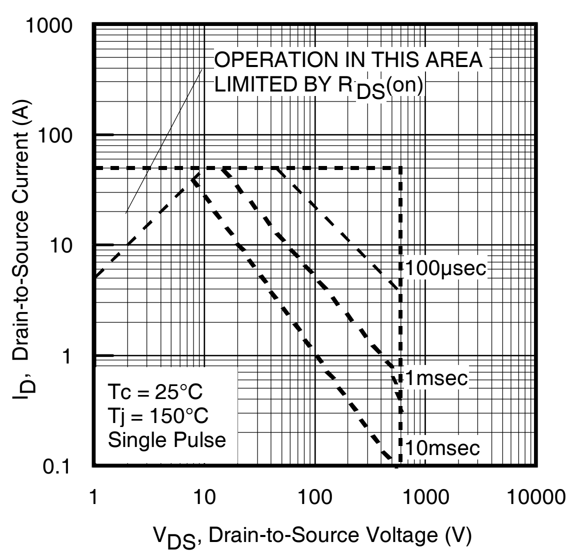


Fig 11. Maximum Safe Operating Area

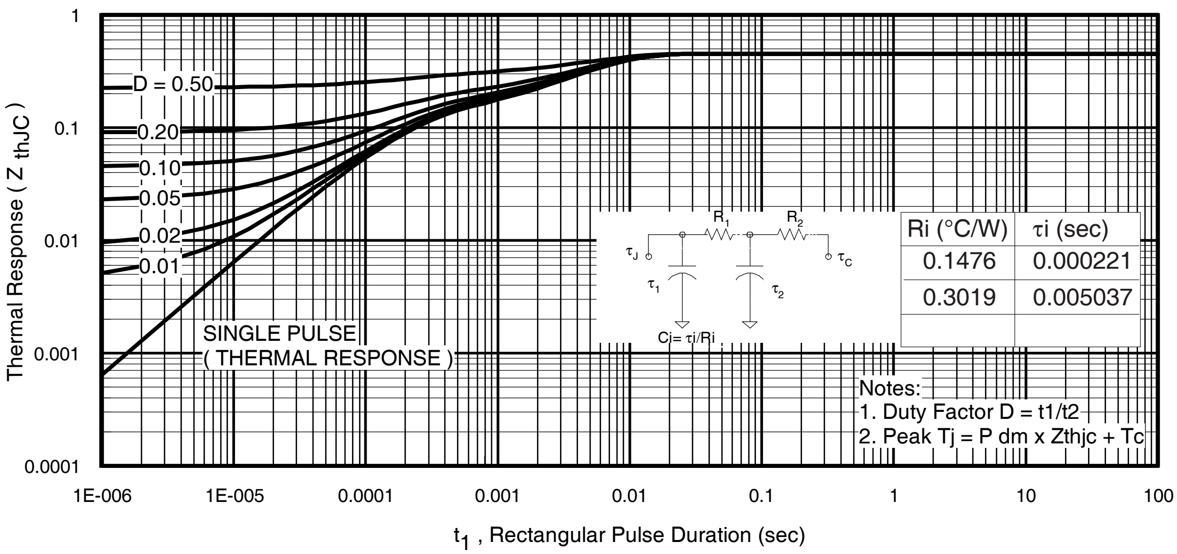


Fig 12. Maximum Effective Transient Thermal Impedance, Junction-to-Case

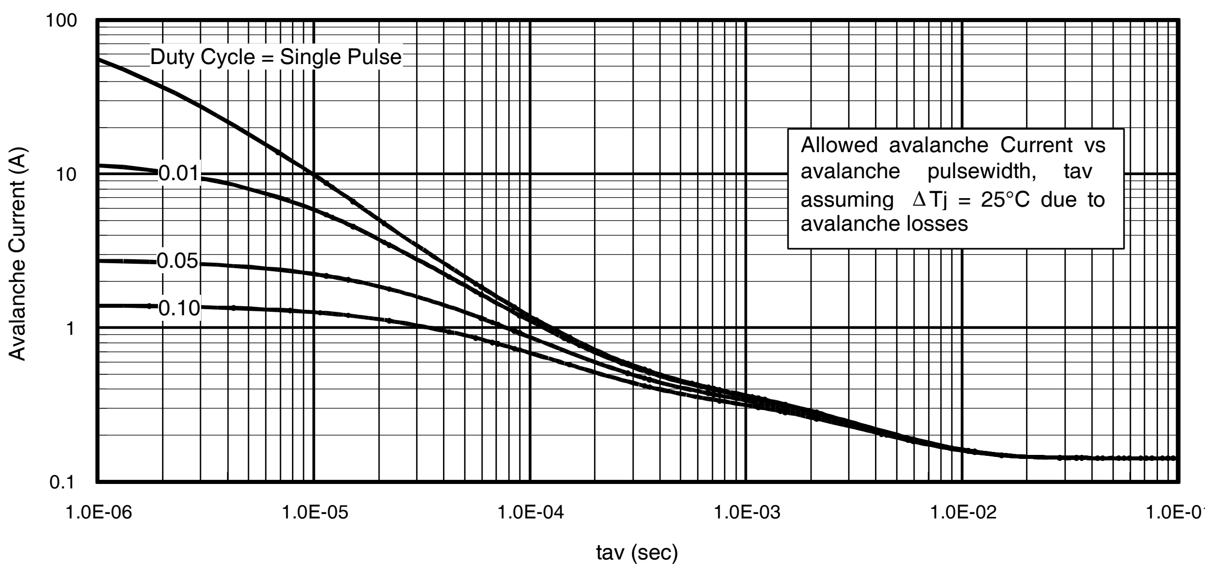


Fig 13. Typical Avalanche Current vs.Pulsewidth

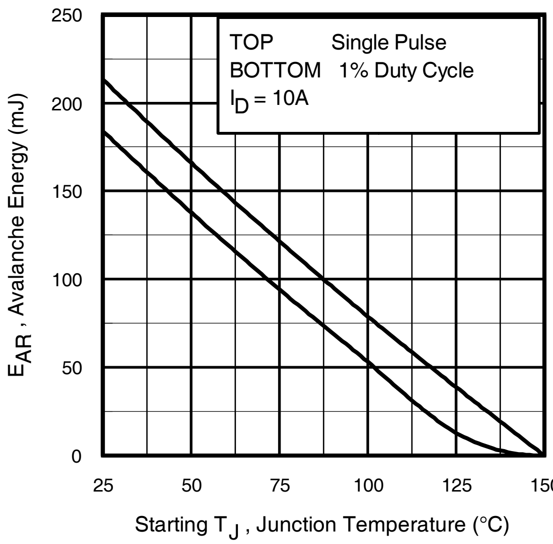


Fig 14. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 13, 14:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figures 12, 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

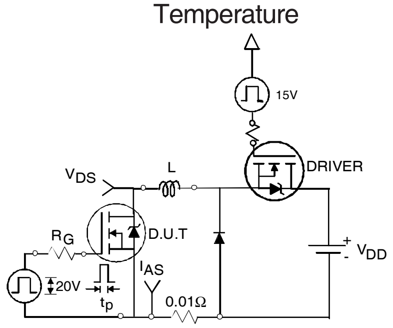


Fig 15a. Unclamped Inductive Test Circuit

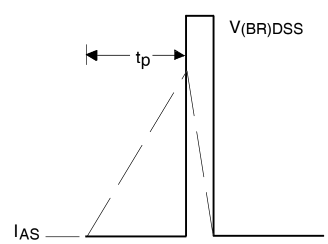


Fig 15b. Unclamped Inductive Waveforms

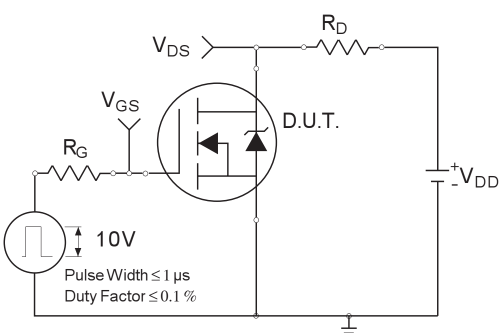


Fig 16a. Switching Time Test Circuit

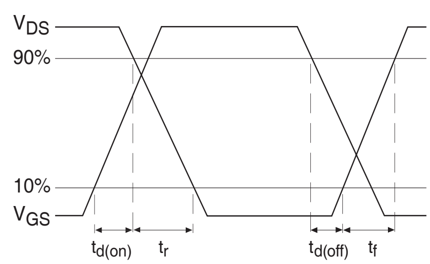


Fig 16b. Switching Time Waveforms

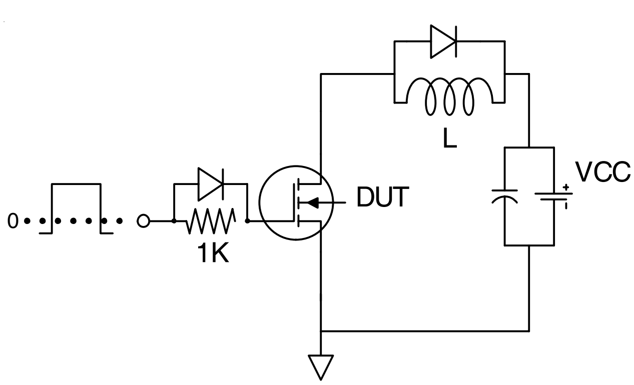


Fig 17. Gate Charge Test Circuit

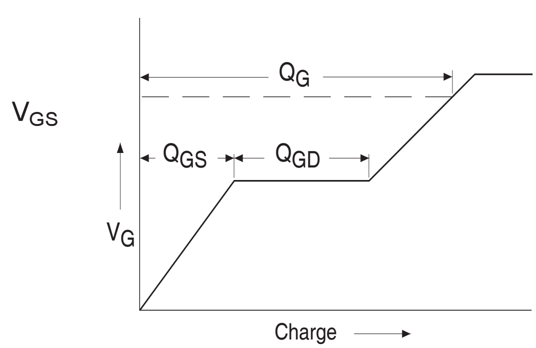


Fig 18. Basic Gate Charge Waveform

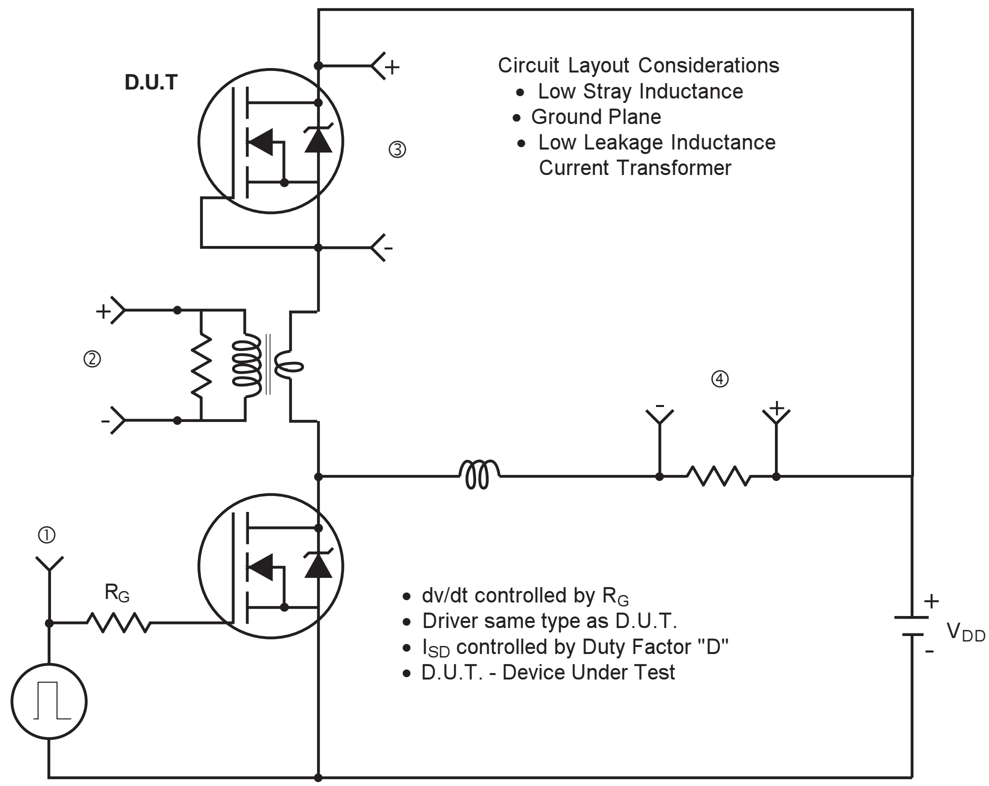
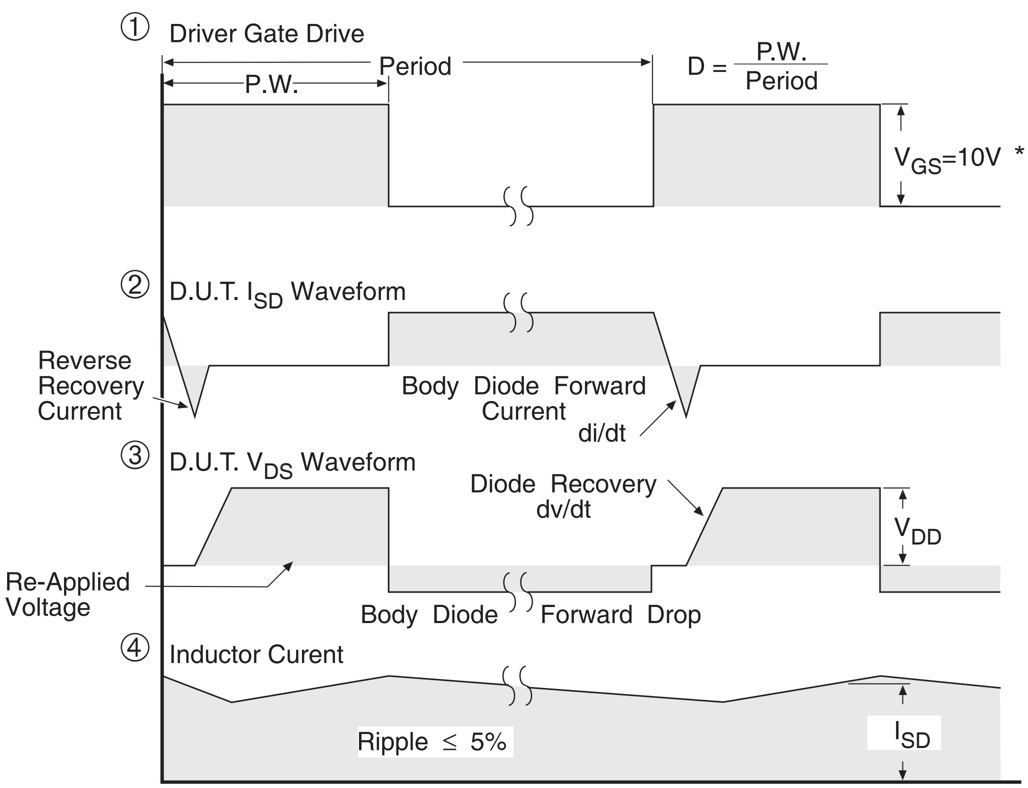


Fig. 19. Peak Diode Recovery dv/dt Test Circuit

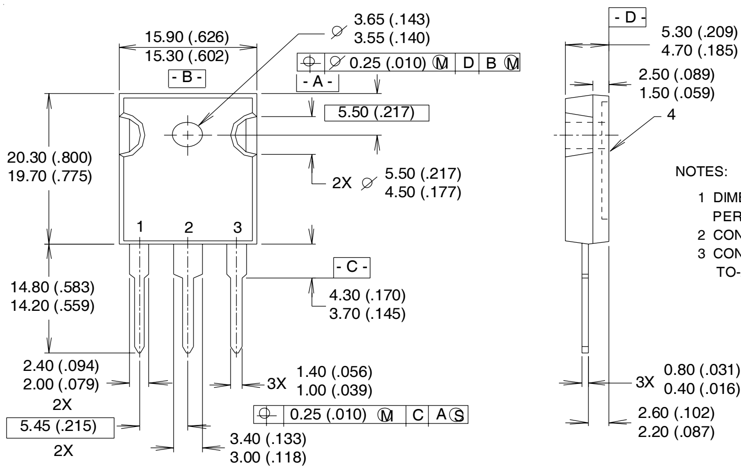


* V_{GS} = 5V for Logic Level Devices

Fig 20. For N-Channel Power MOSFETs

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

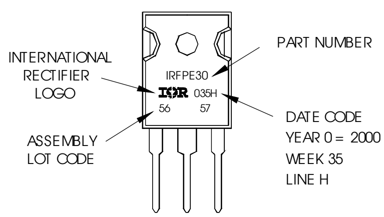
LEAD ASSIGNMENTS

Hexfet	IGBT
1 - Gate	1 - Gate
2 - Drain	2 - Collector
3 - Source	3 - Emitter
4 - Drain	4 - Collector

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



TO-247AC packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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