

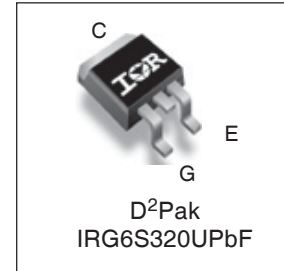
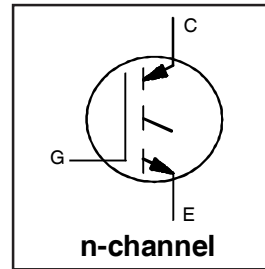
IRG6S320UPbF

Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}^{TM}) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters

$V_{CE\ min}$	330	V
$V_{CE(on)}\ typ.\ @\ I_C = 24A$	1.45	V
$I_{RP}\ max\ @\ T_C = 25^\circ C$	160	A
$T_J\ max$	150	$^\circ C$



G	C	E
Gate	Collector	Emitter

Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}^{TM} rating per silicon area which improve panel efficiency. Additional features are $150^\circ C$ operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	± 30	V
$I_C\ @\ T_C = 25^\circ C$	Continuous Collector Current, $V_{GE}\ @\ 15V$	50 ④	A
$I_C\ @\ T_C = 100^\circ C$	Continuous Collector, $V_{GE}\ @\ 15V$	25	
$I_{RP}\ @\ T_C = 25^\circ C$	Repetitive Peak Current ①	160	
$P_D\ @\ T_C = 25^\circ C$	Power Dissipation	114	W
$P_D\ @\ T_C = 100^\circ C$	Power Dissipation	45	
	Linear Derating Factor	0.91	W/ $^\circ C$
T_J	Operating Junction and	-40 to + 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	1.1	$^\circ C/W$

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{CES}	Collector-to-Emitter Breakdown Voltage	330	—	—	V	V _{GE} = 0V, I _{CE} = 500μA
V _{(BR)ECS}	Emitter-to-Collector Breakdown Voltage③	30	—	—	V	V _{GE} = 0V, I _{CE} = 1 A
ΔBV _{CES} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.30	—	V/°C	Reference to 25°C, I _{CE} = 1mA
V _{CE(on)}	Static Collector-to-Emitter Voltage	—	1.20	—	V	V _{GE} = 15V, I _{CE} = 12A ③
		—	1.45	1.65		V _{GE} = 15V, I _{CE} = 24A ③
		—	1.95	—		V _{GE} = 15V, I _{CE} = 48A ③
		—	2.20	—		V _{GE} = 15V, I _{CE} = 60A ③
		—	2.26	—		V _{GE} = 15V, I _{CE} = 48A, T _J = 150°C ③
V _{GE(th)}	Gate Threshold Voltage	2.6	—	5.0	V	V _{CE} = V _{GE} , I _{CE} = 250μA
ΔV _{GE(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-10	—	mV/°C	
I _{CES}	Collector-to-Emitter Leakage Current	—	1.0	10	μA	V _{CE} = 330V, V _{GE} = 0V
		—	5.0	—		V _{CE} = 330V, V _{GE} = 0V, T _J = 100°C
		—	20	100		V _{CE} = 330V, V _{GE} = 0V, T _J = 125°C
		—	75	—		V _{CE} = 330V, V _{GE} = 0V, T _J = 150°C
I _{GES}	Gate-to-Emitter Forward Leakage	—	—	100	nA	V _{GE} = 30V
	Gate-to-Emitter Reverse Leakage	—	—	-100		V _{GE} = -30V
g _{fe}	Forward Transconductance	—	28	—	S	V _{CE} = 25V, I _{CE} = 12A
Q _g	Total Gate Charge	—	46	—	nC	V _{CE} = 200V, I _C = 12A, V _{GE} = 15V③
Q _{gc}	Gate-to-Collector Charge	—	7.7	—		
t _{d(on)}	Turn-On delay time	—	24	—	ns	I _C = 12A, V _{CC} = 196V R _G = 10Ω, L=210μH, L _S = 150nH T _J = 25°C
t _r	Rise time	—	20	—		
t _{d(off)}	Turn-Off delay time	—	89	—		
t _f	Fall time	—	70	—		
t _{d(on)}	Turn-On delay time	—	23	—	ns	I _C = 12A, V _{CC} = 196V R _G = 10Ω, L=200μH, L _S = 150nH T _J = 150°C
t _r	Rise time	—	52	—		
t _{d(off)}	Turn-Off delay time	—	130	—		
t _f	Fall time	—	140	—		
t _{st}	Shoot Through Blocking Time	100	—	—	ns	V _{CC} = 240V, V _{GE} = 15V, R _G = 5.1Ω
E _{PULSE}	Energy per Pulse	—	240	—	μJ	L = 220nH, C= 0.10μF, V _{GE} = 15V V _{CC} = 240V, R _G = 5.1Ω, T _J = 25°C
		—	280	—		L = 220nH, C= 0.10μF, V _{GE} = 15V V _{CC} = 240V, R _G = 5.1Ω, T _J = 100°C
ESD	Human Body Model	Class 2 (Per JEDEC standard JESD22-A114)				
	Machine Model	Class B (Per EIA/JEDEC standard EIA/JESD22-A115)				
C _{ies}	Input Capacitance	—	1160	—	pF	V _{GE} = 0V
C _{oes}	Output Capacitance	—	61	—		V _{CE} = 30V
C _{res}	Reverse Transfer Capacitance	—	38	—		f = 1.0MHz, See Fig.13
L _C	Internal Collector Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.)
L _E	Internal Emitter Inductance	—	13	—		from package and center of die contact

Notes:

- ① Half sine wave with duty cycle ≤ 0.05 , $t_{on} = 2\mu\text{sec}$.
- ② R_θ is measured at T_J of approximately 90°C .
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.

④ Packaging limitation for this device is 42A.

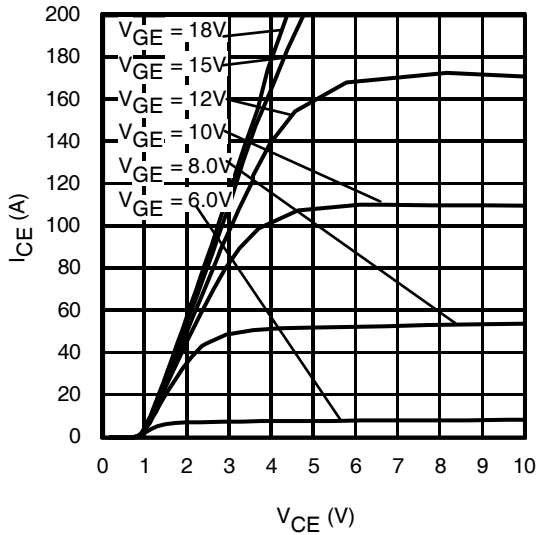


Fig 1. Typical Output Characteristics @ 25°C

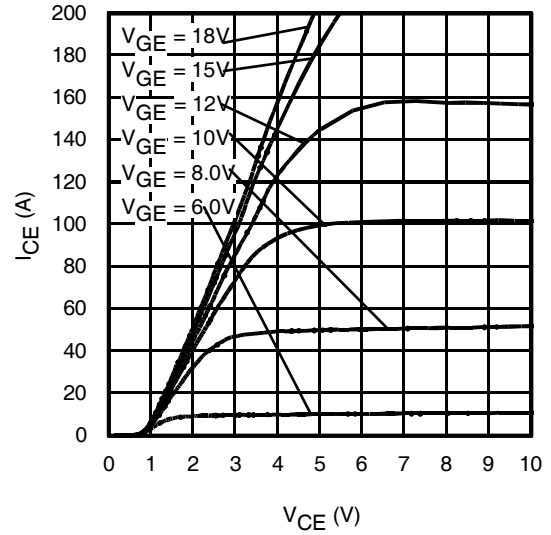


Fig 2. Typical Output Characteristics @ 75°C

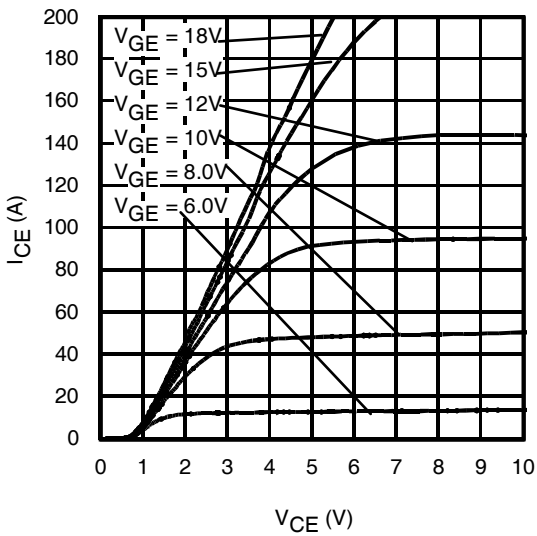


Fig 3. Typical Output Characteristics @ 125°C

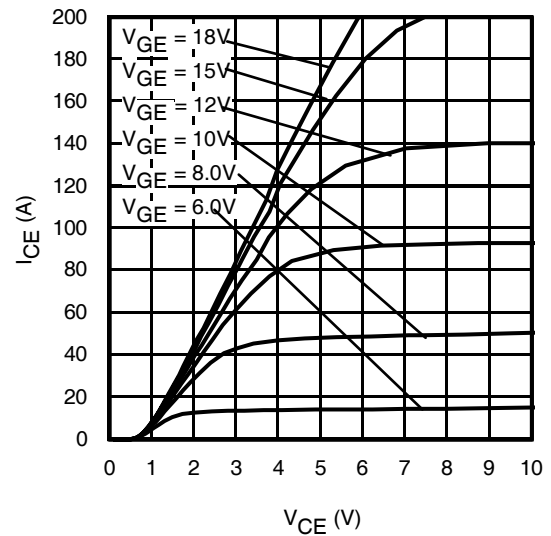


Fig 4. Typical Output Characteristics @ 150°C

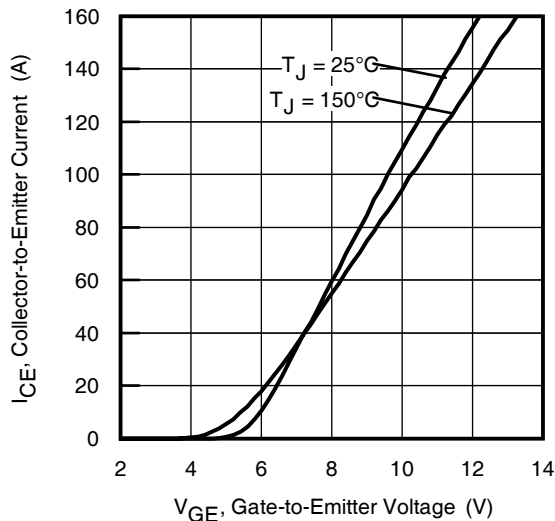


Fig 5. Typical Transfer Characteristics

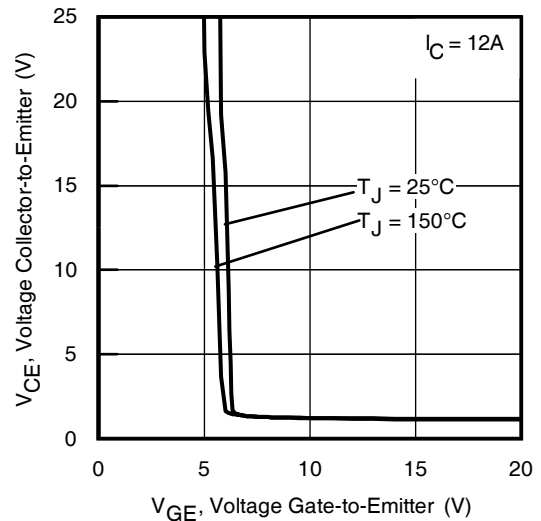


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

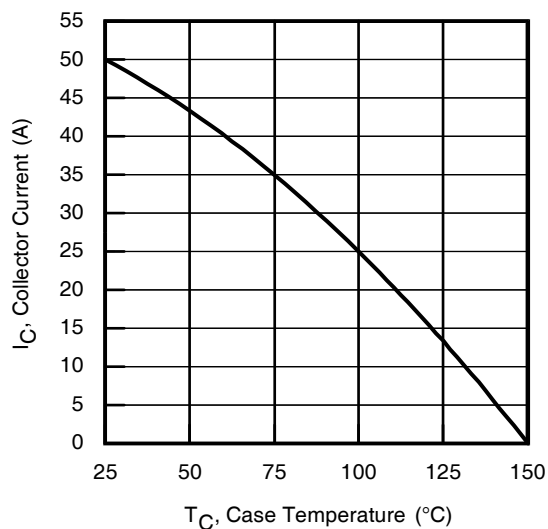


Fig 7. Maximum Collector Current vs. Case Temperature

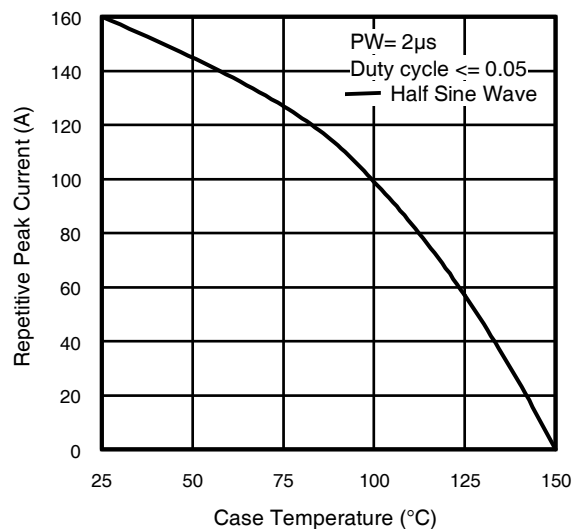


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

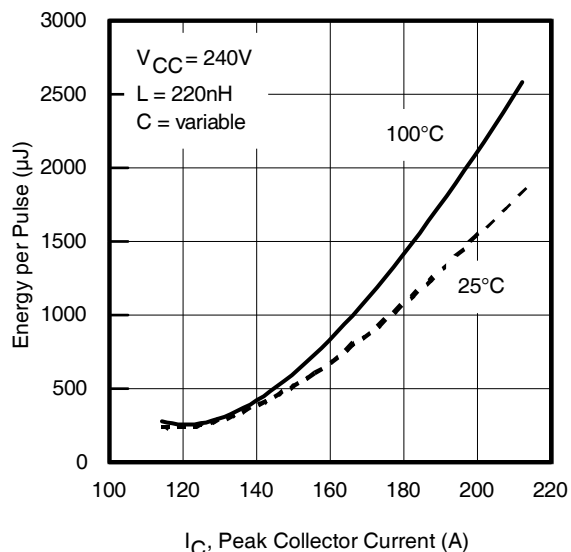


Fig 9. Typical E_{PULSE} vs. Collector Current

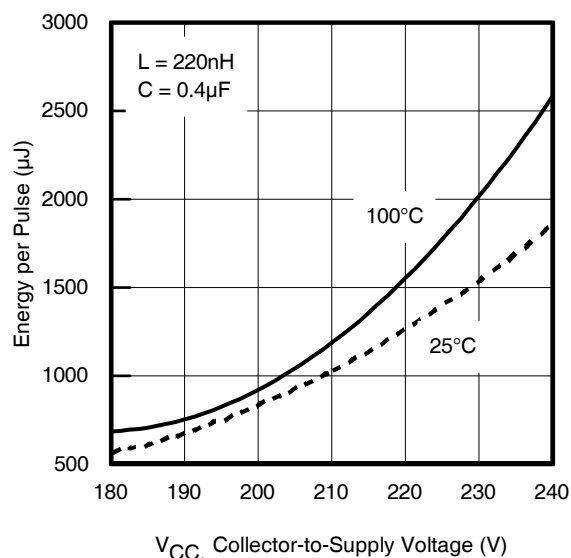


Fig 10. Typical E_{PULSE} vs. Collector-to-Supply Voltage

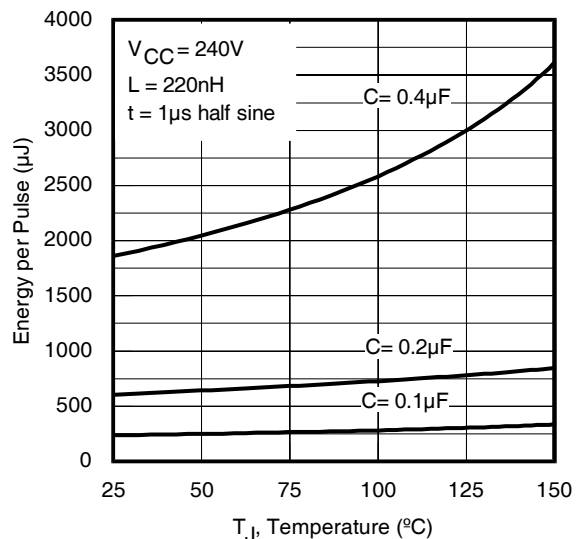


Fig 11. E_{PULSE} vs. Temperature

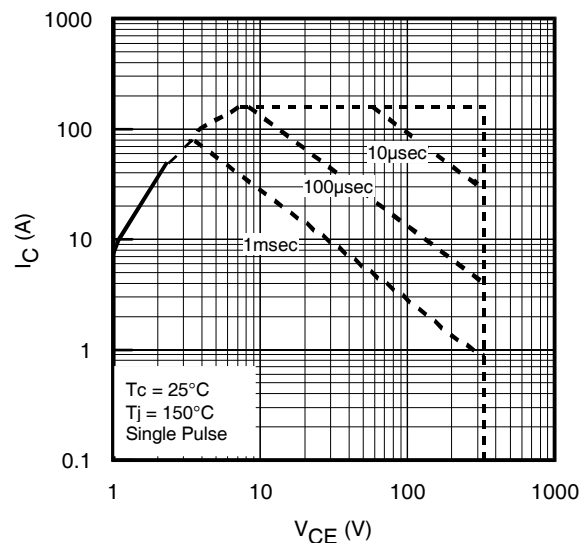


Fig 12. Forward Bias Safe Operating Area

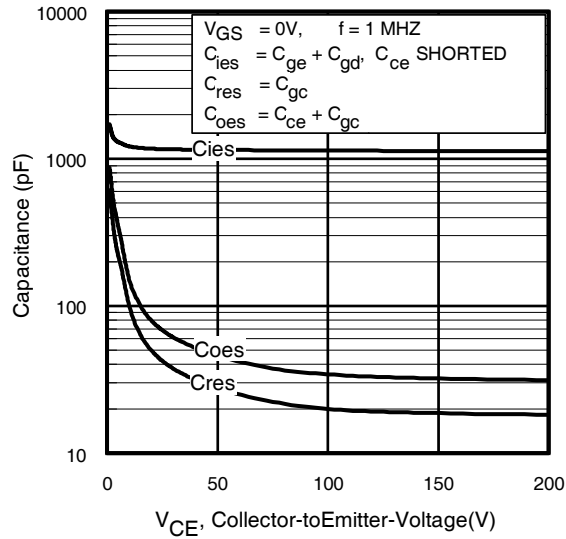


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

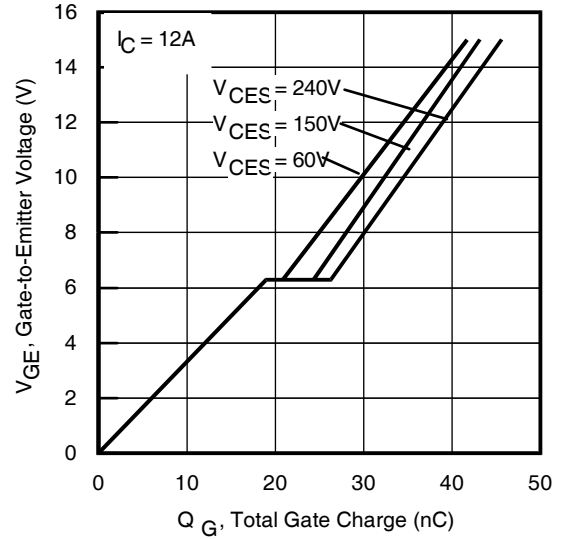


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

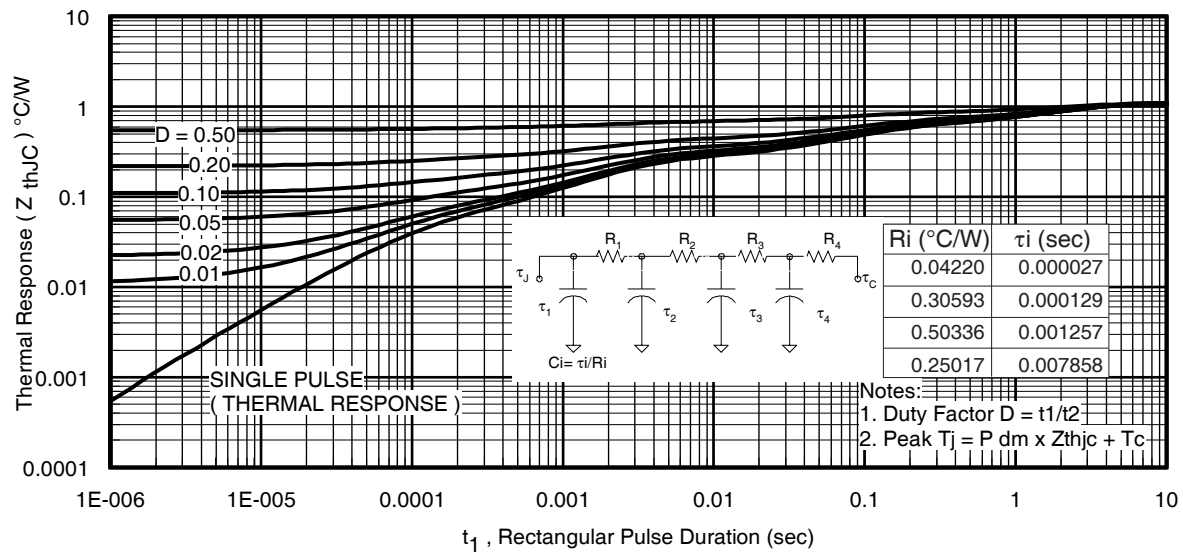


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

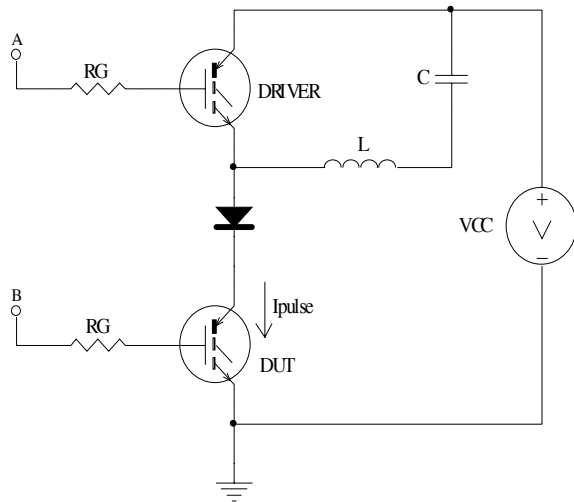


Fig 16a. t_{st} and E_{PULSE} Test Circuit

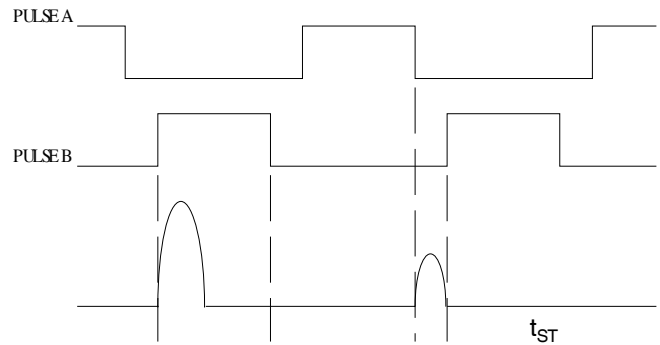


Fig 16b. t_{st} Test Waveforms

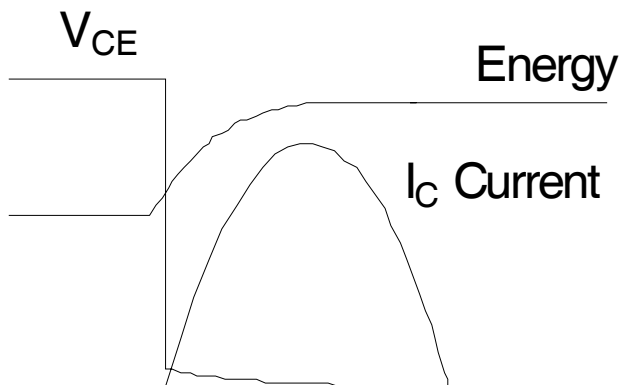


Fig 16c. E_{PULSE} Test Waveforms

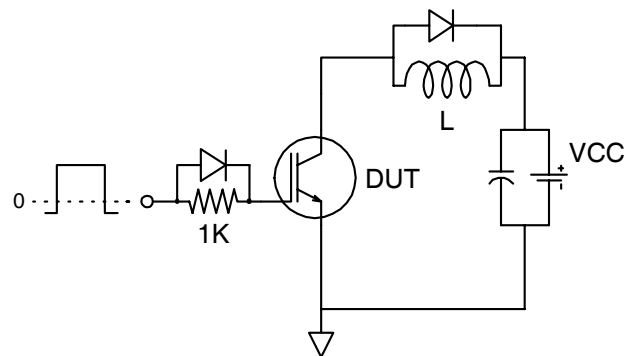
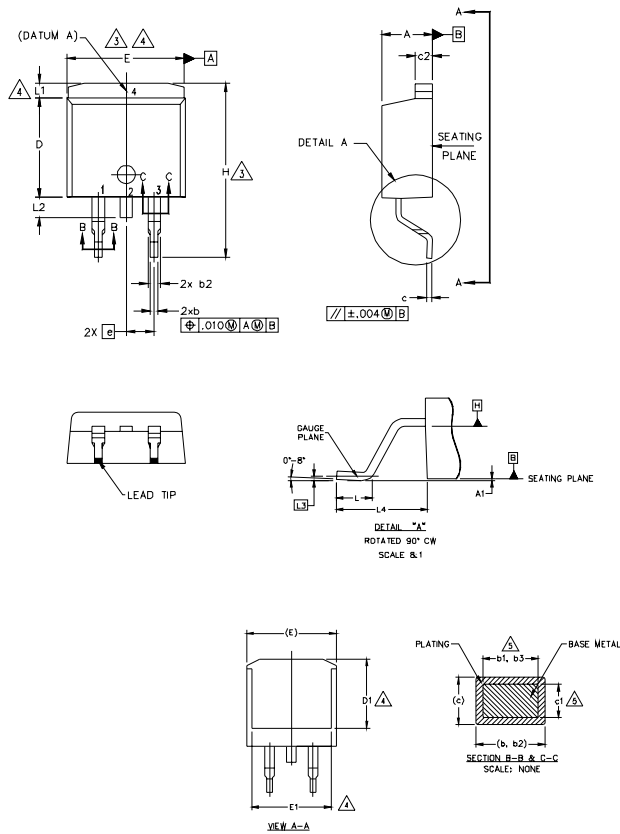


Fig. 17 - Gate Charge Circuit (turn-off)

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	4
L2	1.27	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1. - GATE
- 2, 4. - DRAIN
3. - SOURCE

IGBTs, CoPACK

1. - GATE
- 2, 4. - COLLECTOR
3. - EMITTER

DIODES

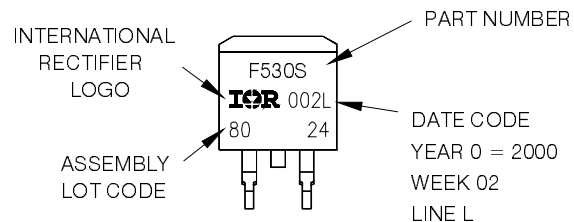
1. - ANODE *
- 2, 4. - CATHODE
3. - ANODE

* PART DEPENDENT.

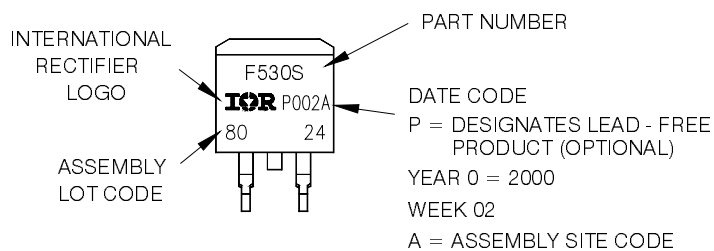
D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position
indicates "Lead - Free"



OR



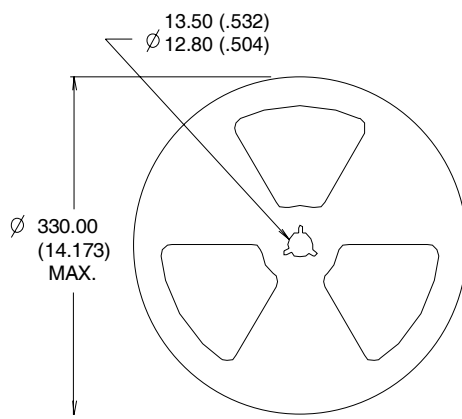
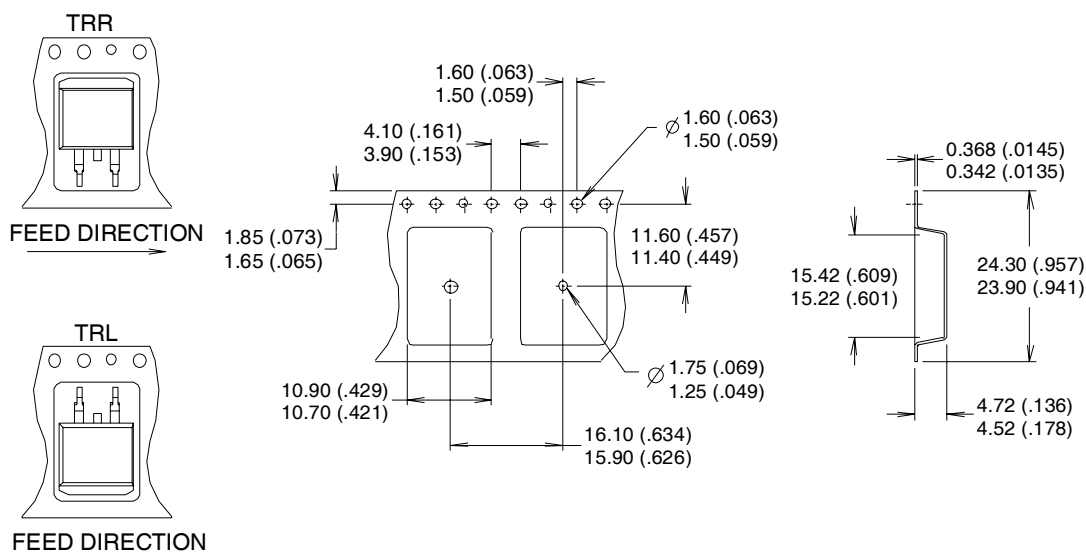
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

IRG6S320UPbF

International
IR Rectifier

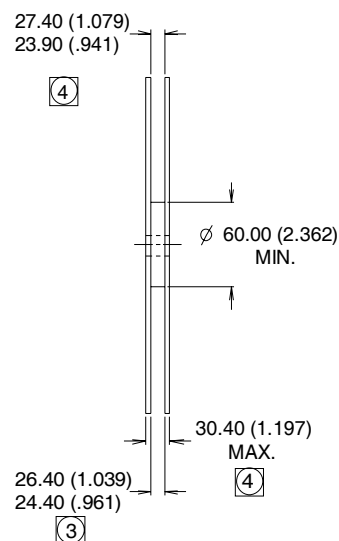
D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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