

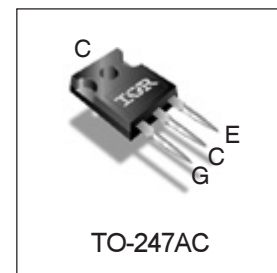
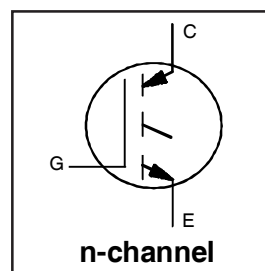
IRG7PA19UPbF

Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}^{TM}) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

Key Parameters

$V_{CE\ min}$	360	V
$V_{CE(on)}\ typ.\ @\ I_C = 30A$	1.49	V
$I_{RP}\ max\ @\ T_C = 25^{\circ}C$	300	A
$T_J\ max$	150	$^{\circ}C$



G	C	E
Gate	Collector	Emitter

Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}^{TM} rating per silicon area which improve panel efficiency. Additional features are $150^{\circ}C$ operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	± 30	V
$I_C\ @\ T_C = 25^{\circ}C$	Continuous Collector Current, $V_{GE}\ @\ 15V$	50	A
$I_C\ @\ T_C = 100^{\circ}C$	Continuous Collector, $V_{GE}\ @\ 15V$	26	
$I_{NOMINAL}$	Nominal Current	15	
$I_{RP}\ @\ T_C = 25^{\circ}C$	Repetitive Peak Current ①	300	
$P_D\ @\ T_C = 25^{\circ}C$	Power Dissipation	104	W
$P_D\ @\ T_C = 100^{\circ}C$	Power Dissipation	42	
	Linear Derating Factor	0.83	W/ $^{\circ}C$
T_J	Operating Junction and	-40 to + 150	$^{\circ}C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	1.2	$^{\circ}C/W$
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	—	40	
Wt	Weight	6.0	—	g

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{CES}	Collector-to-Emitter Breakdown Voltage	360	—	—	V	V _{GE} = 0V, I _{CE} = 250μA
ΔBV _{CES} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.34	—	V/°C	Reference to 25°C, I _{CE} = 1mA
V _{CE(on)}	Static Collector-to-Emitter Voltage	—	1.26	1.52	V	V _{GE} = 15V, I _{CE} = 15A ③
		—	1.41	—		V _{GE} = 15V, I _{CE} = 25A ③
		—	1.49	—		V _{GE} = 15V, I _{CE} = 30A ③
		—	1.65	—		V _{GE} = 15V, I _{CE} = 40A ③
		—	2.12	—		V _{GE} = 15V, I _{CE} = 70A ③
		—	2.93	—		V _{GE} = 15V, I _{CE} = 120A ③
		—	1.51	—		V _{GE} = 15V, I _{CE} = 25A, T _J = 150°C ③
		V _{GE(th)}	Gate Threshold Voltage	2.2		—
ΔV _{GE(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-10	—	mV/°C	
I _{CES}	Collector-to-Emitter Leakage Current	—	1.0	20	μA	V _{CE} = 360V, V _{GE} = 0V
		—	35	200		V _{CE} = 360V, V _{GE} = 0V, T _J = 125°C
		—	130	—		V _{CE} = 360V, V _{GE} = 0V, T _J = 150°C
I _{GES}	Gate-to-Emitter Forward Leakage	—	—	100	nA	V _{GE} = 30V
	Gate-to-Emitter Reverse Leakage	—	—	-100		V _{GE} = -30V
g _{fe}	Forward Transconductance	—	62	—	S	V _{CE} = 25V, I _{CE} = 25A
Q _g	Total Gate Charge	—	38	—	nC	V _{CE} = 200V, I _C = 25A, V _{GE} = 15V③
Q _{gc}	Gate-to-Collector Charge	—	12	—		
t _{d(on)}	Turn-On delay time	—	15	—	ns	I _C = 25A, V _{CC} = 196V R _G = 10Ω, L = 200μH, L _S = 150nH T _J = 25°C
t _r	Rise time	—	21	—		
t _{d(off)}	Turn-Off delay time	—	68	—		
t _f	Fall time	—	88	—		
t _{d(on)}	Turn-On delay time	—	15	—	ns	I _C = 25A, V _{CC} = 196V R _G = 10Ω, L = 200μH, L _S = 150nH T _J = 150°C
t _r	Rise time	—	23	—		
t _{d(off)}	Turn-Off delay time	—	84	—		
t _f	Fall time	—	191	—		
t _{st}	Shoot Through Blocking Time	100	—	—	ns	V _{CC} = 240V, V _{GE} = 15V, R _G = 5.1Ω
E _{PULSE}	Energy per Pulse	—	854	—	μJ	L = 220nH, C = 0.40μF, V _{GE} = 15V V _{CC} = 240V, R _G = 5.1Ω, T _J = 25°C
		—	1083	—		L = 220nH, C = 0.40μF, V _{GE} = 15V V _{CC} = 240V, R _G = 5.1Ω, T _J = 100°C
ESD	Human Body Model	Class 1C (Per JEDEC standard JESD22-A114)				
	Machine Model	Class B (Per EIA/JEDEC standard EIA/JESD22-A115)				
C _{ies}	Input Capacitance	—	1100	—	pF	V _{GE} = 0V
C _{oes}	Output Capacitance	—	57	—		V _{CE} = 30V
C _{res}	Reverse Transfer Capacitance	—	30	—		f = 1.0MHz
L _C	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L _E	Internal Emitter Inductance	—	7.5	—		from package and center of die contact

Notes:

- ① Half sine wave with duty cycle ≤ 0.05 , $t_{on}=2\mu sec$.
- ② R_q is measured at T_J of approximately 90°C .
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

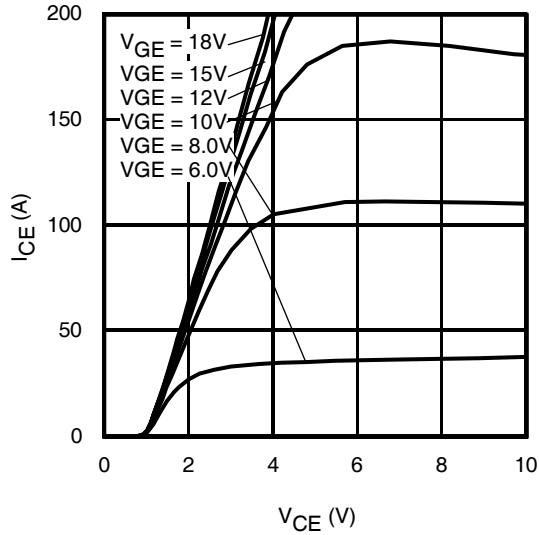


Fig 1. Typical Output Characteristics @ 25°C

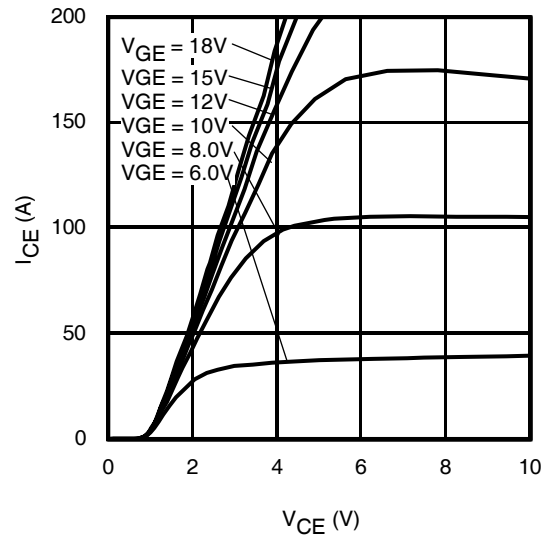


Fig 2. Typical Output Characteristics @ 75°C

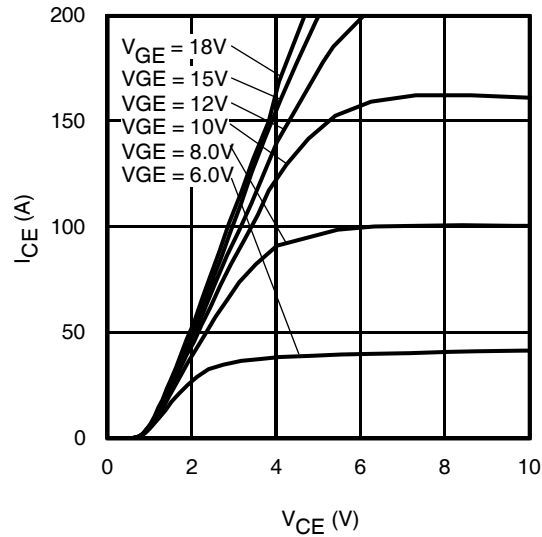


Fig 3. Typical Output Characteristics @ 125°C

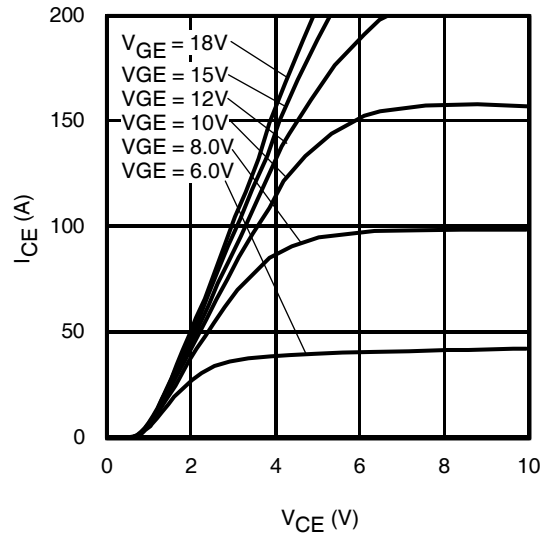


Fig 4. Typical Output Characteristics @ 150°C

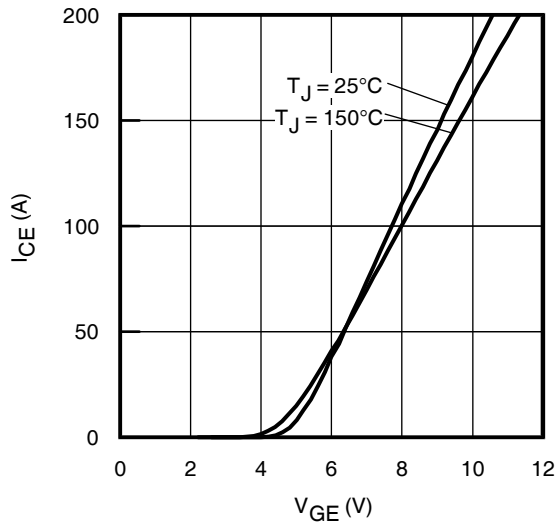


Fig 5. Typical Transfer Characteristics

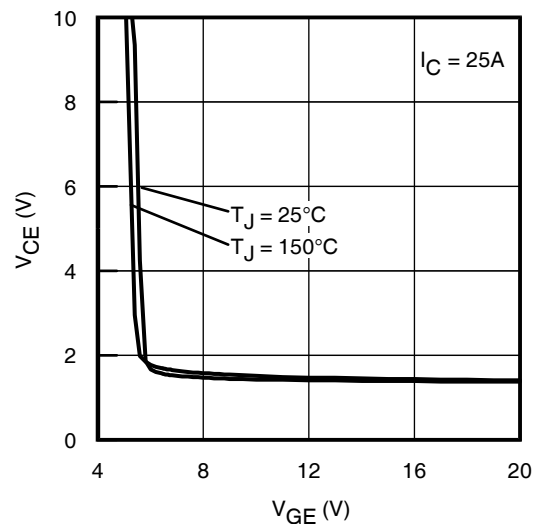


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

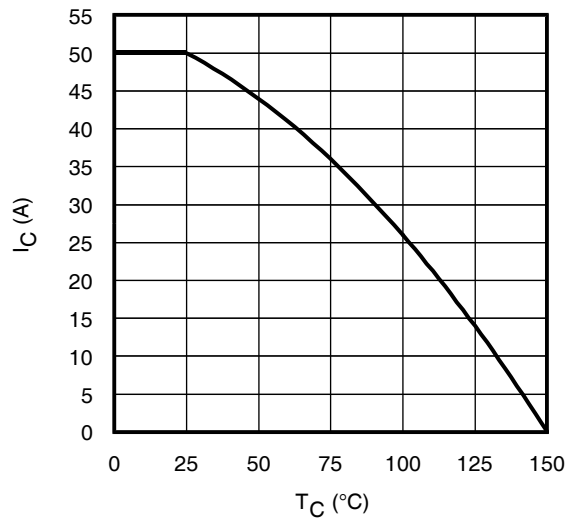


Fig 7. Maximum Collector Current vs. Case Temperature

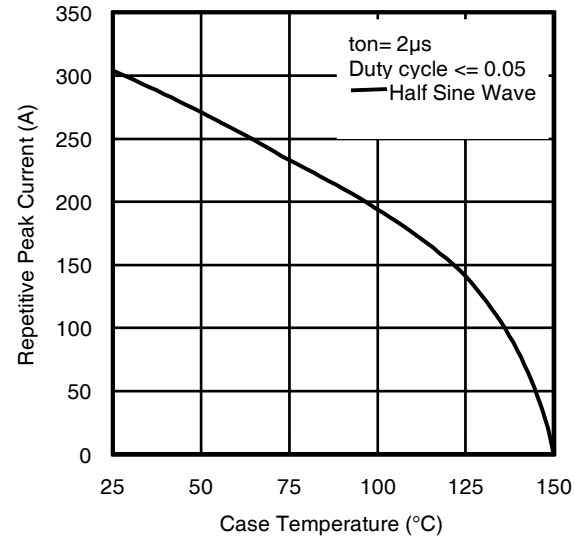


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

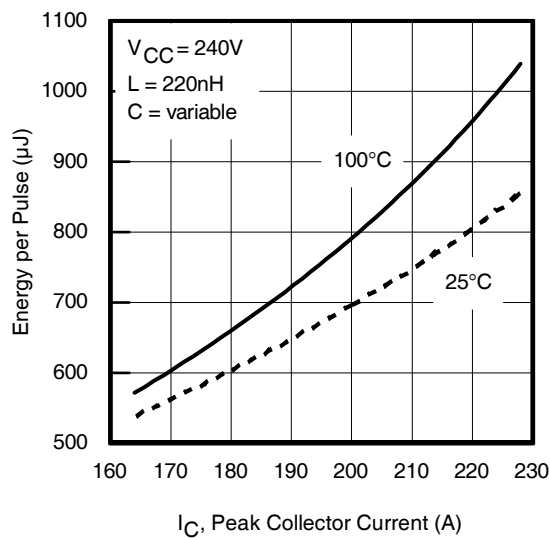


Fig 9. Typical E_{PULSE} vs. Collector Current

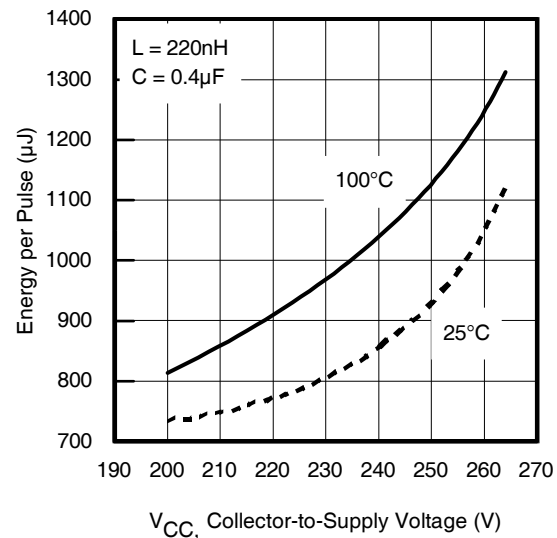


Fig 10. Typical E_{PULSE} vs. Collector-to-Supply Voltage

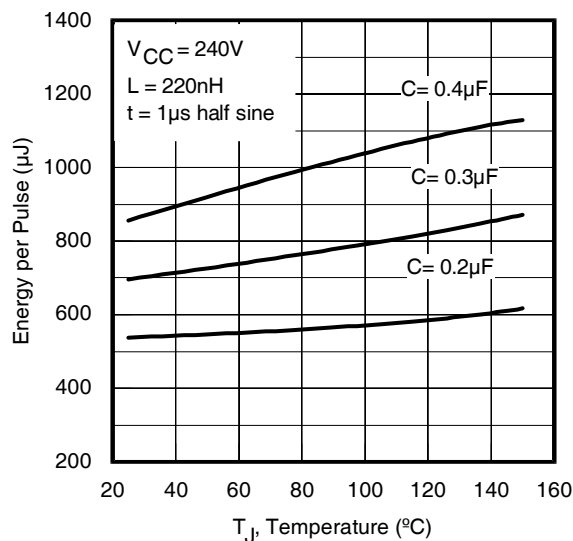


Fig 11. E_{PULSE} vs. Temperature

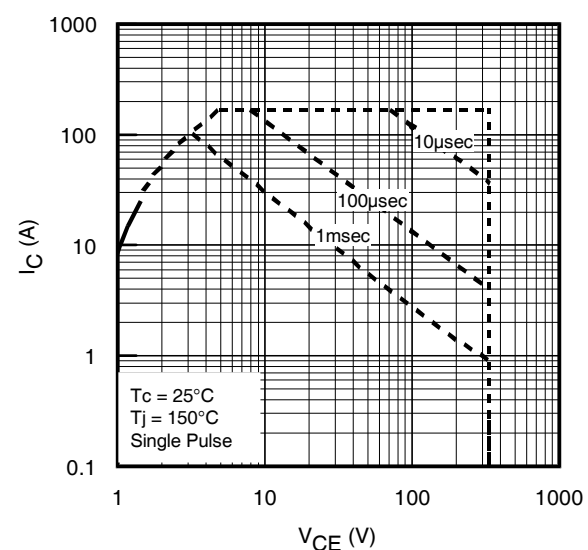


Fig 12. Forward Bias Safe Operating Area

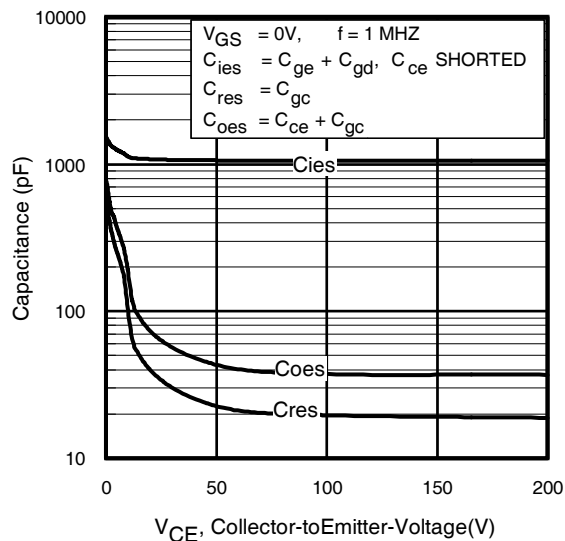


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

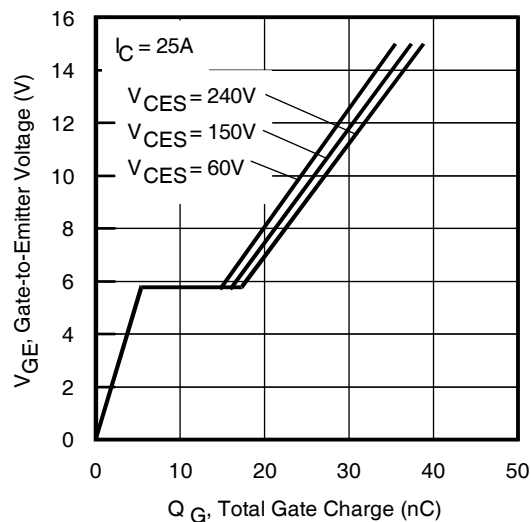


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

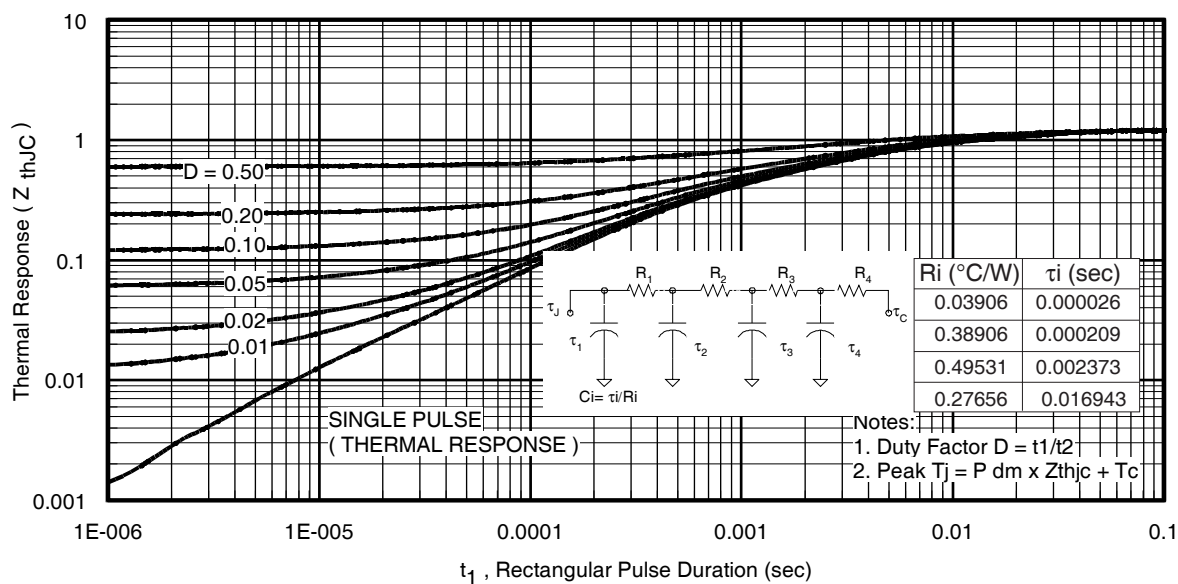


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

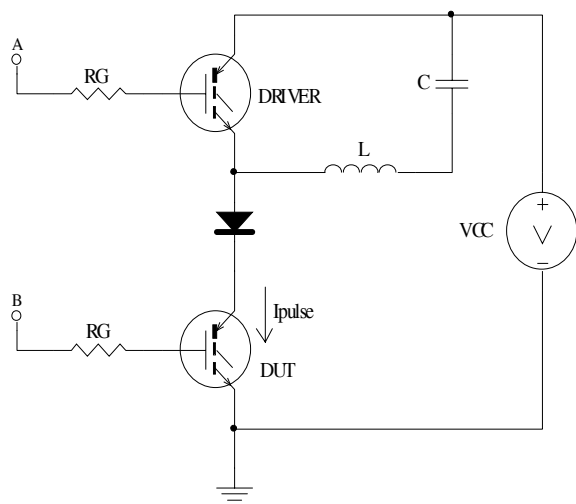


Fig 16a. t_{st} and E_{PULSE} Test Circuit

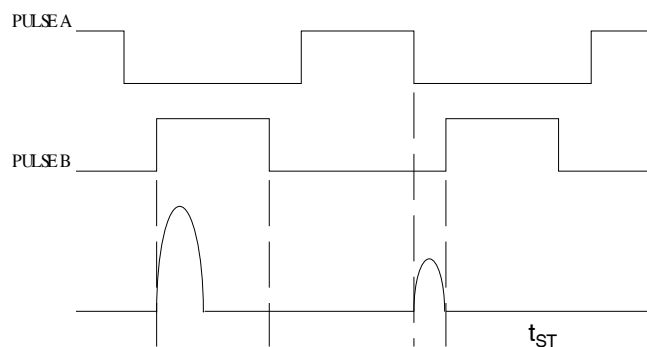


Fig 16b. t_{st} Test Waveforms

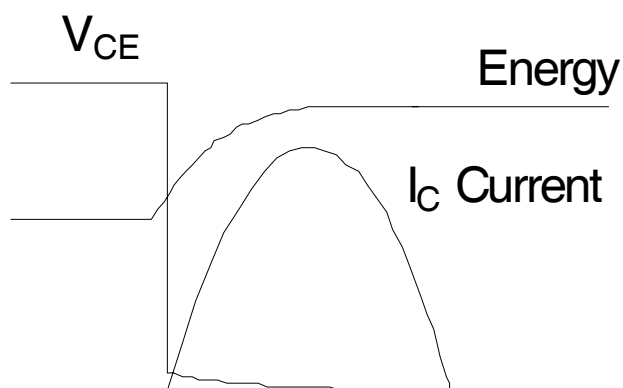
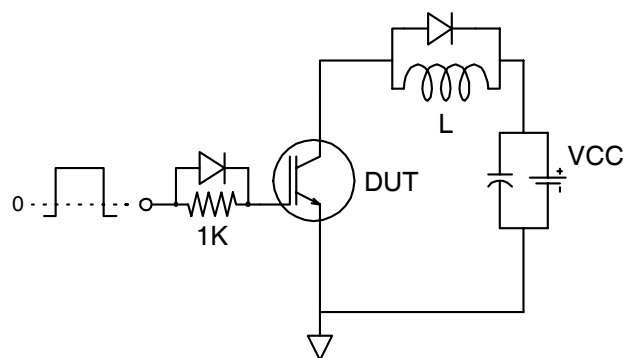
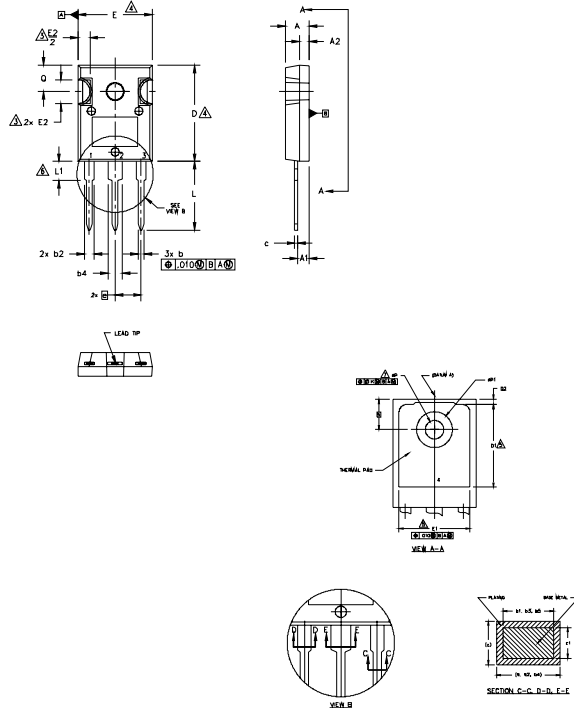


Fig 16c. E_{PULSE} Test Waveforms



TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH; MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTE
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØPI	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

IGBTs, CoPACK

1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

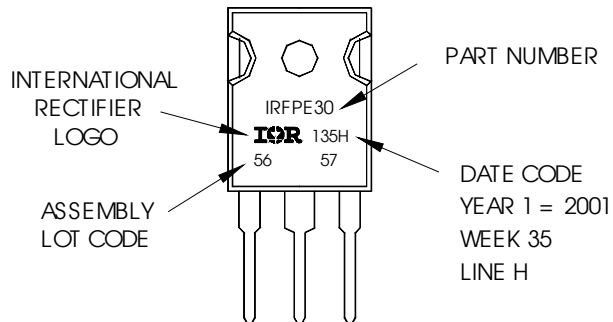
DIODES

1. ANODE/OPEN
2. CATHODE
3. ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed for the Industrial market.
Qualification Standards can be found on IR's Web site.