

INSULATED GATE BIPOLAR TRANSISTOR

Features

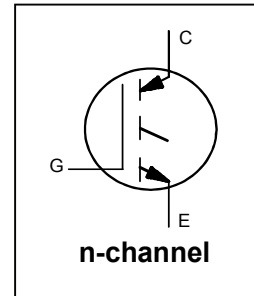
- Low $V_{CE(ON)}$ trench IGBT technology
- Low switching losses
- Square RBSOA
- 100% of the parts tested for I_{LM} ①
- Positive $V_{CE(ON)}$ temperature co-efficient
- Tight parameter distribution
- Lead-free package

Benefits

- High efficiency in a wide range of applications
- Suitable for a wide range of switching frequencies due to low $V_{CE(ON)}$ and low switching losses
- Rugged transient performance for increased reliability
- Excellent current sharing in parallel operation

Applications

- U.P.S.
- Welding
- Solar Inverter
- Induction heating

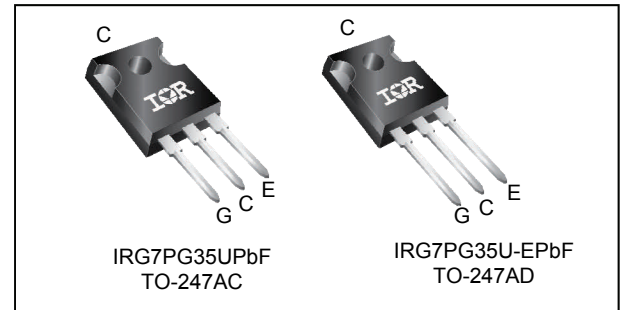


$$V_{CES} = 1000V$$

$$I_C = 35A, T_C = 100^\circ C$$

$$T_{J(MAX)} = 175^\circ C$$

$$V_{CE(ON)} \text{ typ.} = 1.9V @ I_C = 20A$$



G	C	E
Gate	Collector	Emitter

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRG7PG35UPbF	TO-247AC	Tube	25	IRG7PG35UPbF
IRG7PG35U-EPbF	TO-247AD	Tube	25	IRG7PG35U-EPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	1000	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current (Silicon Limited)	55	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current (Silicon Limited)	35	
I_{CM}	Pulse Collector Current, $V_{GE} = 15V$ ②	60	
I_{LM}	Clamped Inductive Load Current, $V_{GE} = 20V$ ①	80	
V_{GE}	Continuous Gate-to-Emitter Voltage	± 30	V
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	210	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	105	
T_J	Operating Junction and	-55 to +175	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in.(1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N-m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Junction-to-Case (IGBT) ④	—	—	0.70	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink (flat, greased surface)	—	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient (typical socket mount)	—	—	40	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1000	—	—	V	$V_{GE} = 0\text{V}$, $I_C = 100\mu\text{A}$ ③
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	1.2	—	V/°C	$V_{GE} = 0\text{V}$, $I_C = 1.0\text{mA}$ (25°C-150°C)
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.9	2.2	V	$I_C = 20\text{A}$, $V_{GE} = 15\text{V}$, $T_J = 25^\circ\text{C}$
		—	2.3	—		$I_C = 20\text{A}$, $V_{GE} = 15\text{V}$, $T_J = 150^\circ\text{C}$
		—	2.4	—		$I_C = 20\text{A}$, $V_{GE} = 15\text{V}$, $T_J = 175^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0	V	$V_{CE} = V_{GE}$, $I_C = 600\mu\text{A}$
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage temp coefficient.	—	-16	—	mV/°C	$V_{CE} = V_{GE}$, $I_C = 600\mu\text{A}$ (25°C-150°C)
g_{fe}	Forward Transconductance	—	22	—	S	$V_{CE} = 50\text{V}$, $I_C = 20\text{A}$, $PW = 30\mu\text{s}$
I_{CES}	Collector-to-Emitter Leakage Current	—	2.0	100	μA	$V_{GE} = 0\text{V}$, $V_{CE} = 1000\text{V}$
		—	2000	—		$V_{GE} = 0\text{V}$, $V_{CE} = 1000\text{V}$, $T_J = 175^\circ\text{C}$
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	$V_{GE} = \pm 30\text{V}$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	—	85	—	nC	$I_C = 20\text{A}$ $V_{GE} = 15\text{V}$ $V_{CC} = 600\text{V}$
Q_{ge}	Gate-to-Emitter Charge	—	15	—		
Q_{gc}	Gate-to-Collector Charge	—	35	—		
E_{on}	Turn-On Switching Loss	—	1060	—	μJ	$I_C = 20\text{A}$, $V_{CC} = 600\text{V}$, $V_{GE} = 15\text{V}$ $R_G = 10\Omega$, $L = 200\mu\text{H}$, $T_J = 25^\circ\text{C}$ Energy losses include tail & diode reverse recovery Diode clamp the same as IRG7PH35UDPbF
E_{off}	Turn-Off Switching Loss	—	620	—		
E_{total}	Total Switching Loss	—	1680	—		
$t_{d(on)}$	Turn-On delay time	—	30	—	ns	Energy losses include tail & diode reverse recovery Diode clamp the same as IRG7PH35UDPbF
t_r	Rise time	—	15	—		
$t_{d(off)}$	Turn-Off delay time	—	160	—		
t_f	Fall time	—	80	—		
E_{on}	Turn-On Switching Loss	—	1880	—	μJ	$I_C = 20\text{A}$, $V_{CC} = 600\text{V}$, $V_{GE} = 15\text{V}$ $R_G = 10\Omega$, $L = 200\mu\text{H}$, $T_J = 175^\circ\text{C}$ Energy losses include tail & diode reverse recovery Diode clamp the same as IRG7PH35UDPbF
E_{off}	Turn-Off Switching Loss	—	1140	—		
E_{total}	Total Switching Loss	—	3020	—		
$t_{d(on)}$	Turn-On delay time	—	25	—	ns	Energy losses include tail & diode reverse recovery Diode clamp the same as IRG7PH35UDPbF
t_r	Rise time	—	20	—		
$t_{d(off)}$	Turn-Off delay time	—	200	—		
t_f	Fall time	—	200	—		
C_{ies}	Input Capacitance	—	1940	—	pF	$V_{GE} = 0\text{V}$ $V_{CC} = 30\text{V}$ $f = 1.0\text{MHz}$
C_{oes}	Output Capacitance	—	60	—		
C_{res}	Reverse Transfer Capacitance	—	40	—		
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 175^\circ\text{C}$, $I_C = 80\text{A}$ $V_{CC} = 800\text{V}$, $V_p \leq 1000\text{V}$ $R_g = 10\Omega$, $V_{GE} = +20\text{V}$ to 0V

Notes:

- ① $V_{CC} = 80\%$ (V_{CES}), $V_{GE} = 20\text{V}$, $R_G = 10\Omega$.
- ② Pulse width limited by max. junction temperature.
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.
- ④ R_θ is measured at T_J of approximately 90°C .

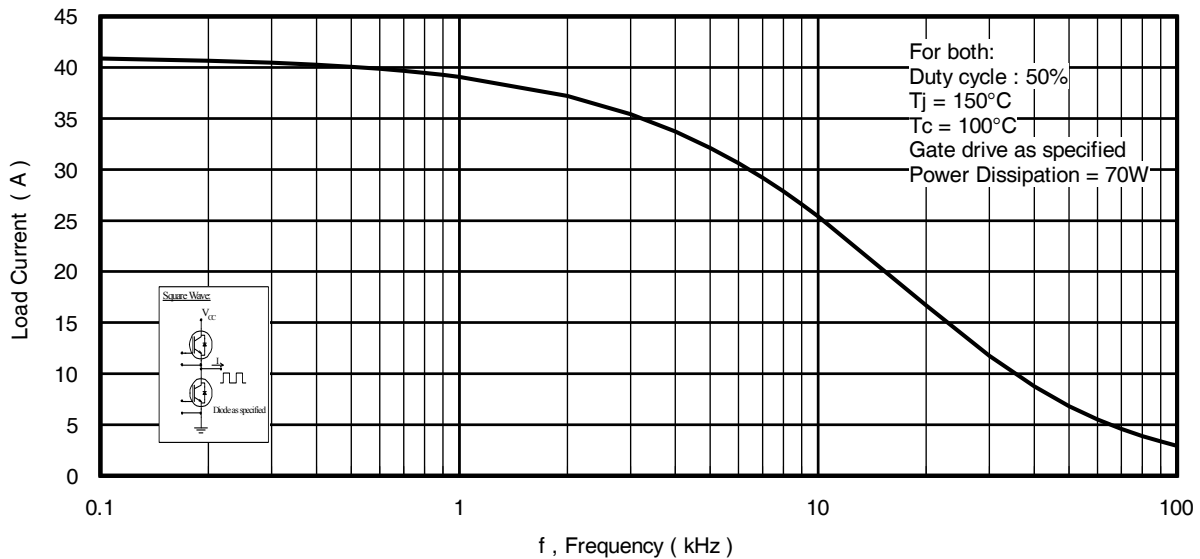


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

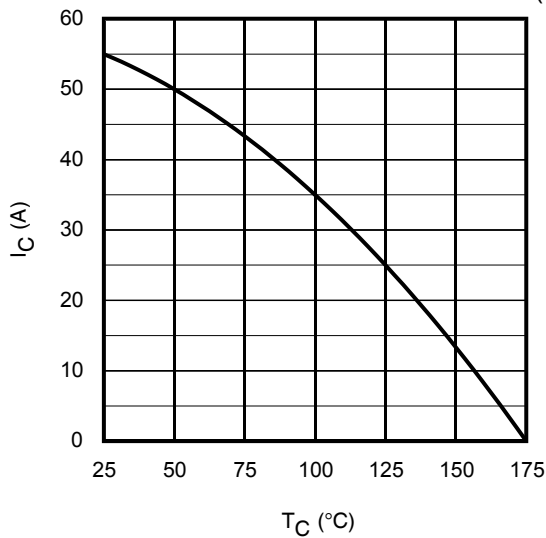


Fig. 2 - Maximum DC Collector Current vs. Case Temperature

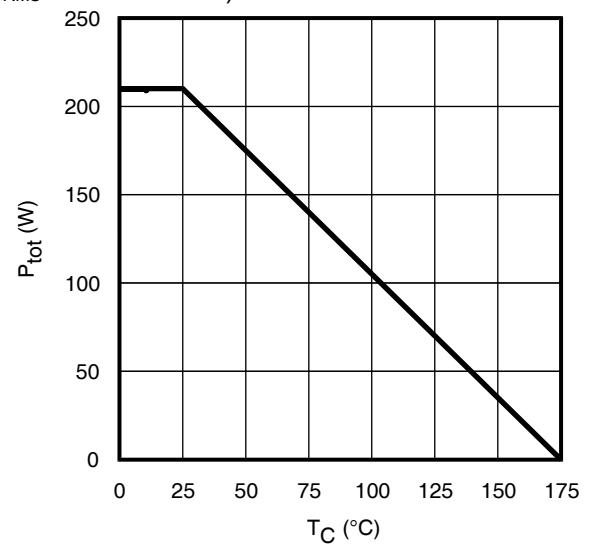


Fig. 3 - Power Dissipation vs. Case Temperature

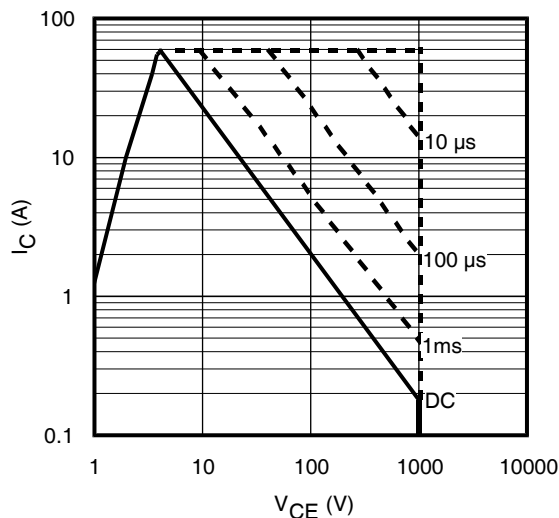


Fig. 4 - Forward SOA
 $T_C = 25^{\circ}\text{C}$, $T_J \leq 175^{\circ}\text{C}$; $V_{\text{GE}} = 15\text{V}$

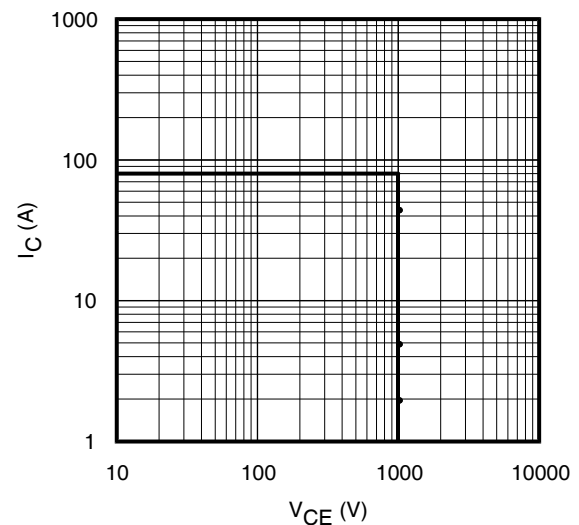


Fig. 5 - Reverse Bias SOA
 $T_J = 175^{\circ}\text{C}$; $V_{\text{GE}} = 20\text{V}$

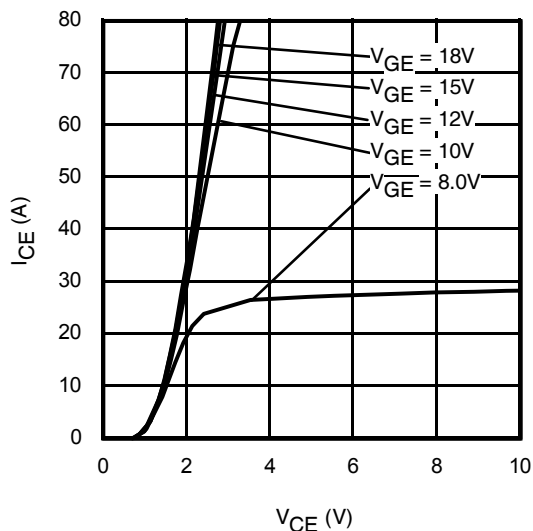


Fig. 6 - Typ. IGBT Output Characteristics
 $T_J = -40^{\circ}\text{C}$; $t_p = 30\mu\text{s}$

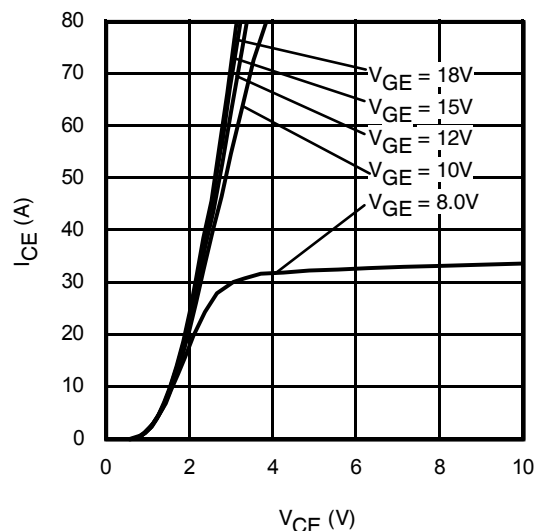


Fig. 7 - Typ. IGBT Output Characteristics
 $T_J = 25^{\circ}\text{C}$; $t_p = 30\mu\text{s}$

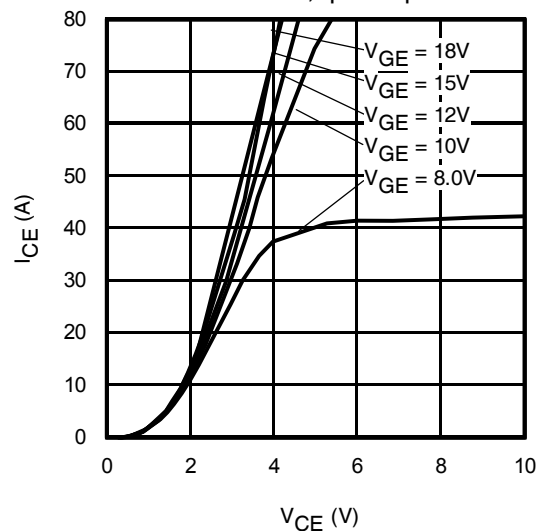


Fig. 8 - Typ. IGBT Output Characteristics
 $T_J = 175^{\circ}\text{C}$; $t_p = 30\mu\text{s}$

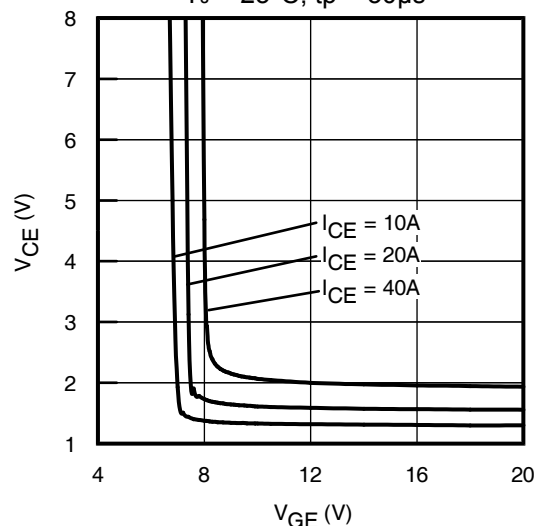


Fig. 9 - Typical V_{CE} vs. V_{GE}
 $T_J = -40^{\circ}\text{C}$

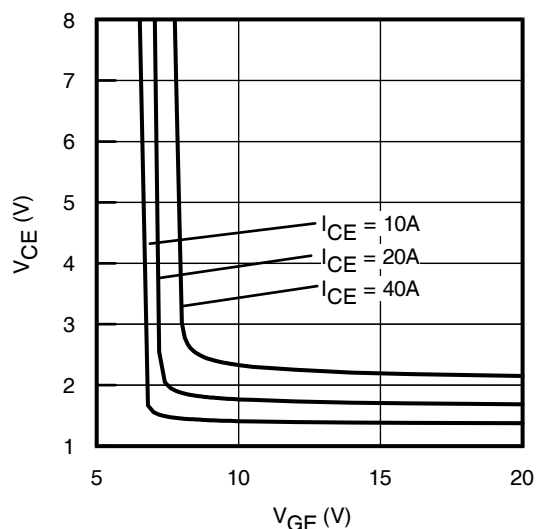


Fig. 10 - Typical V_{CE} vs. V_{GE}
 $T_J = 25^{\circ}\text{C}$

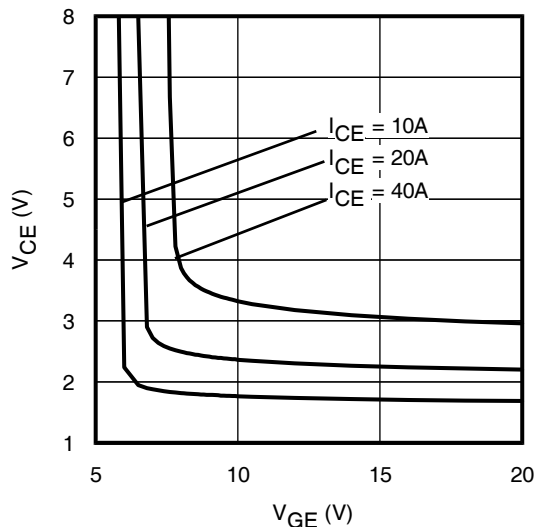


Fig. 11 - Typical V_{CE} vs. V_{GE}
 $T_J = 175^{\circ}\text{C}$

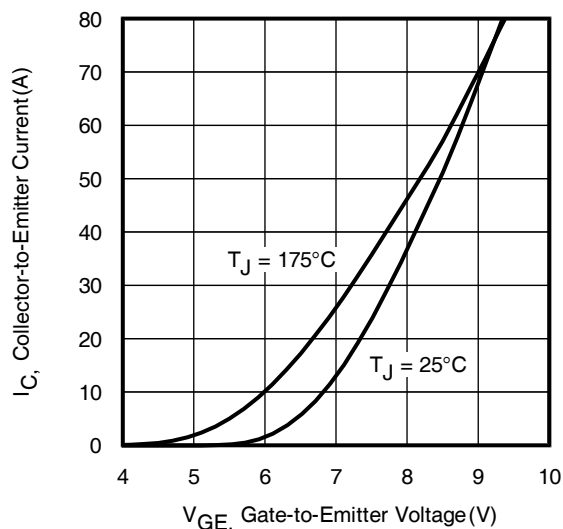


Fig. 12 - Typ. Transfer Characteristics
 $V_{CE} = 50V$; $t_p = 30\mu s$

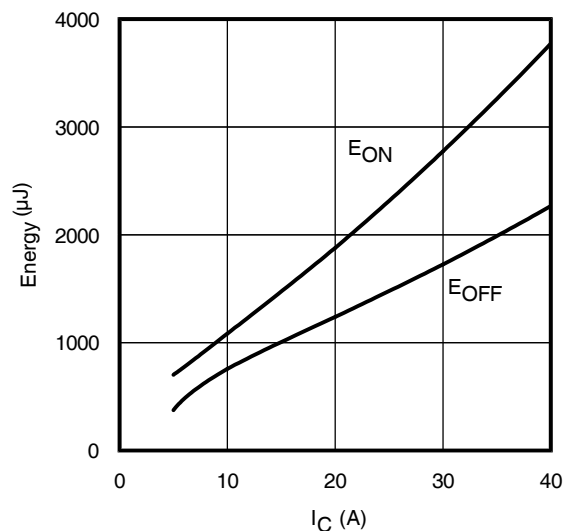


Fig. 13 - Typ. Energy Loss vs. I_C
 $T_J = 175^\circ C$; $L = 680\mu H$; $V_{CE} = 600V$, $R_G = 10\Omega$; $V_{GE} = 15V$

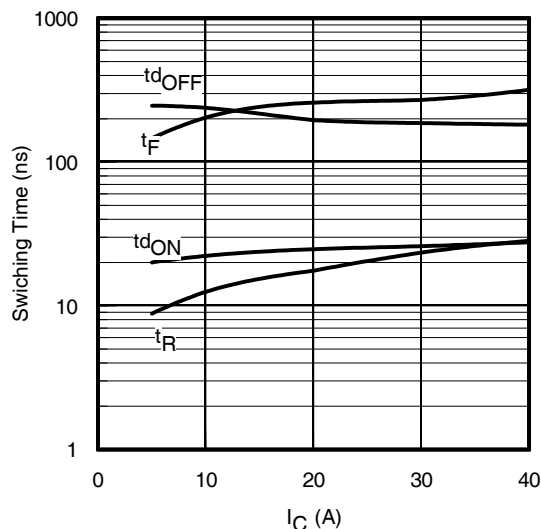


Fig. 14 - Typ. Switching Time vs. I_C
 $T_J = 175^\circ C$; $L = 680\mu H$; $V_{CE} = 600V$, $R_G = 10\Omega$; $V_{GE} = 15V$

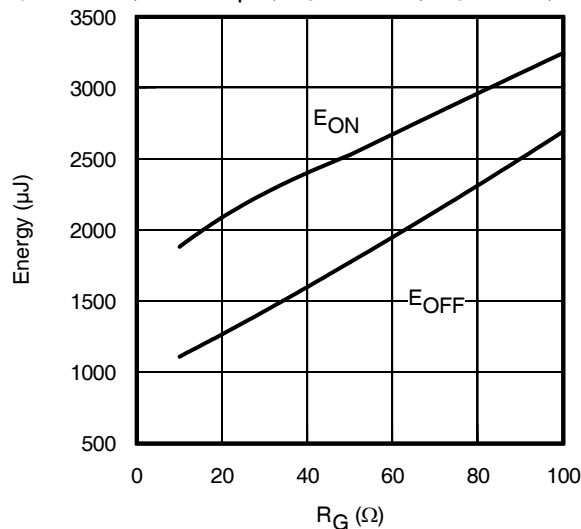


Fig. 15 - Typ. Energy Loss vs. R_G
 $T_J = 175^\circ C$; $L = 680\mu H$; $V_{CE} = 600V$, $I_{CE} = 20A$; $V_{GE} = 15V$

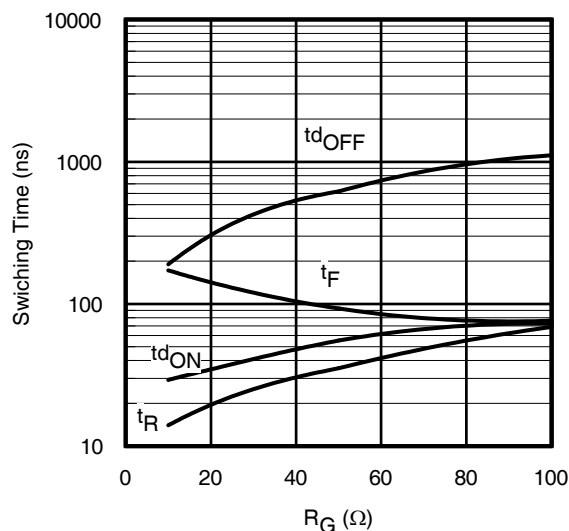


Fig. 16 - Typ. Switching Time vs. R_G
 $T_J = 175^\circ C$; $L = 680\mu H$; $V_{CE} = 600V$, $I_{CE} = 20A$; $V_{GE} = 15V$

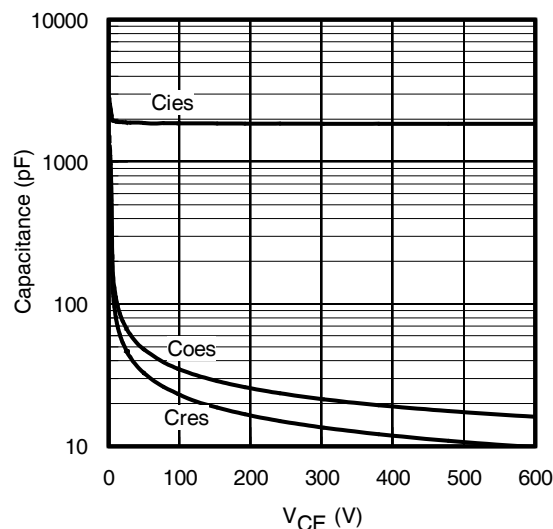


Fig. 17 - Typ. Capacitance vs. V_{CE}
 $V_{GE} = 0V$; $f = 1MHz$

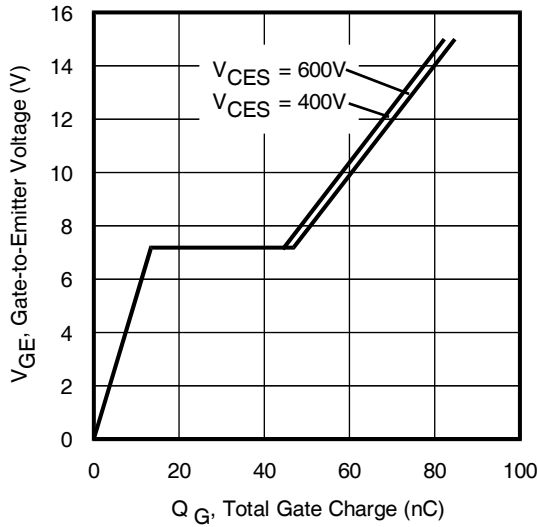


Fig. 18 - Typical Gate Charge vs. V_{GE}
 $I_{CE} = 20A$

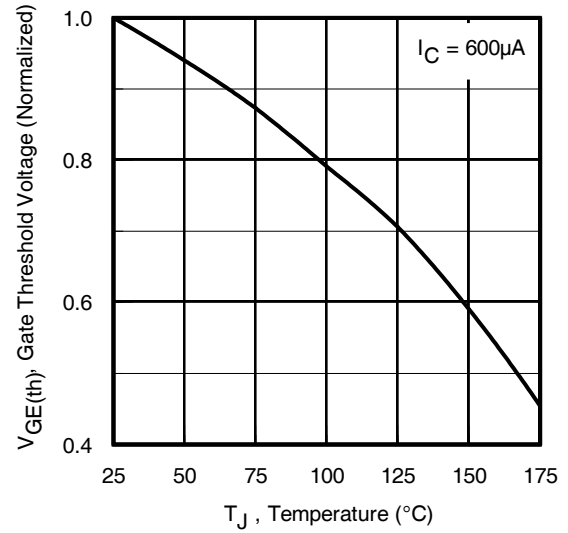


Fig. 19 - Typical Gate Threshold Voltage
 (Normalized) vs. Junction Temperature

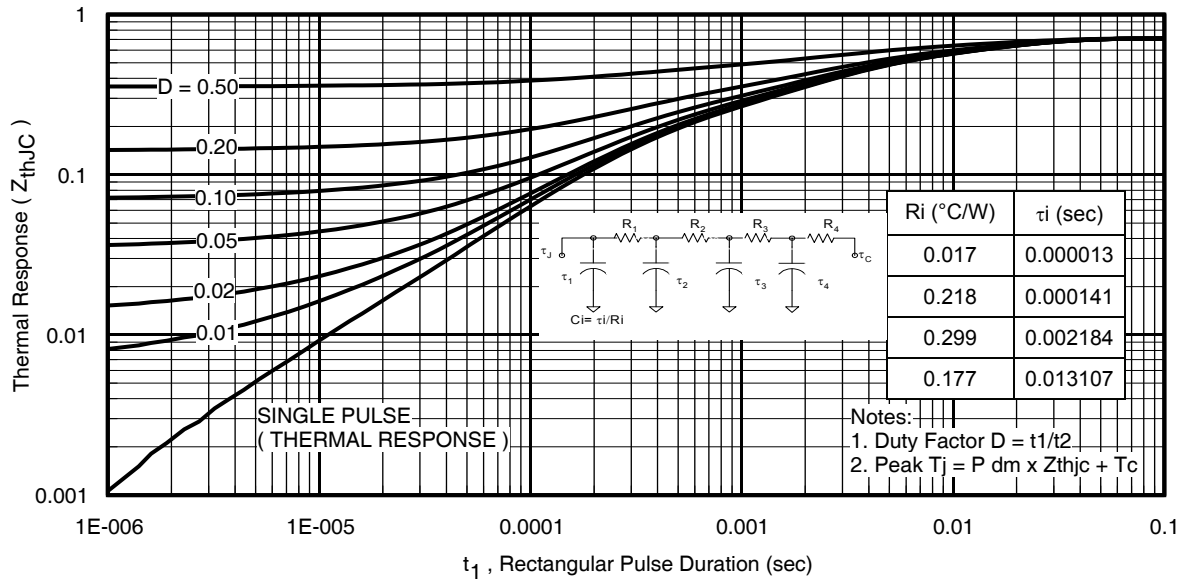
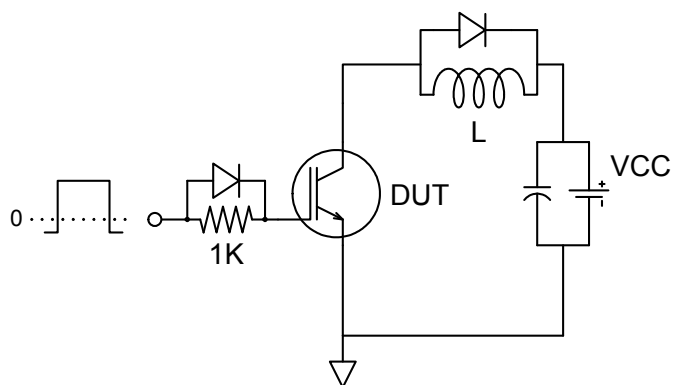
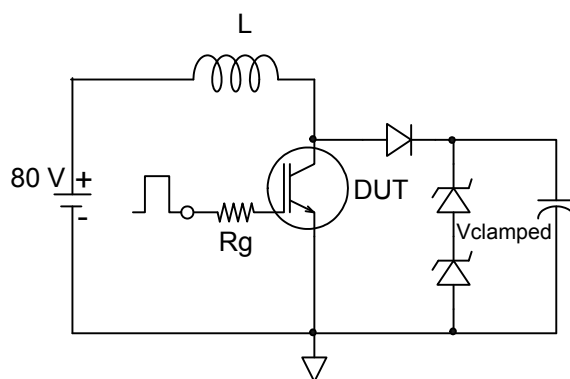
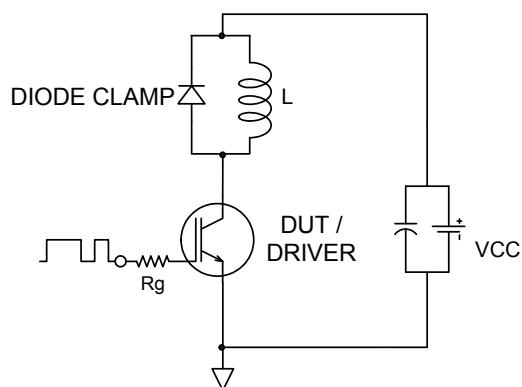
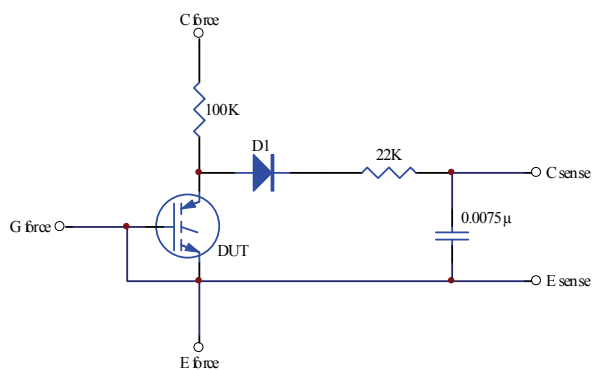


Fig. 20 - Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)


Fig.C.T.1 - Gate Charge Circuit (turn-off)

Fig.C.T.2 - RBSOA Circuit

Fig.C.T.3 - Switching Loss Circuit

Fig.C.T.4 - BVCEs Filter Circuit

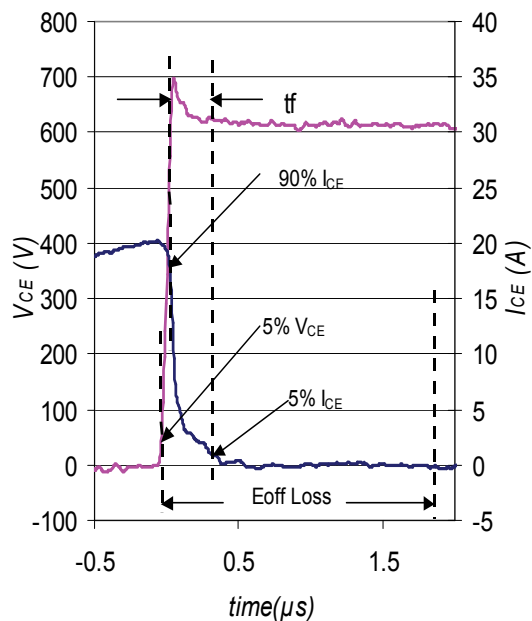


Fig. WF1 - Typ. Turn-off Loss Waveform
@ $T_J = 175^\circ\text{C}$ using Fig. CT.3

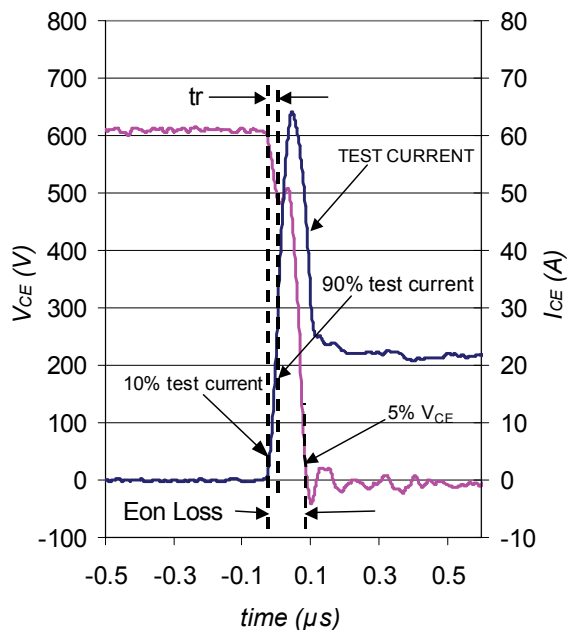
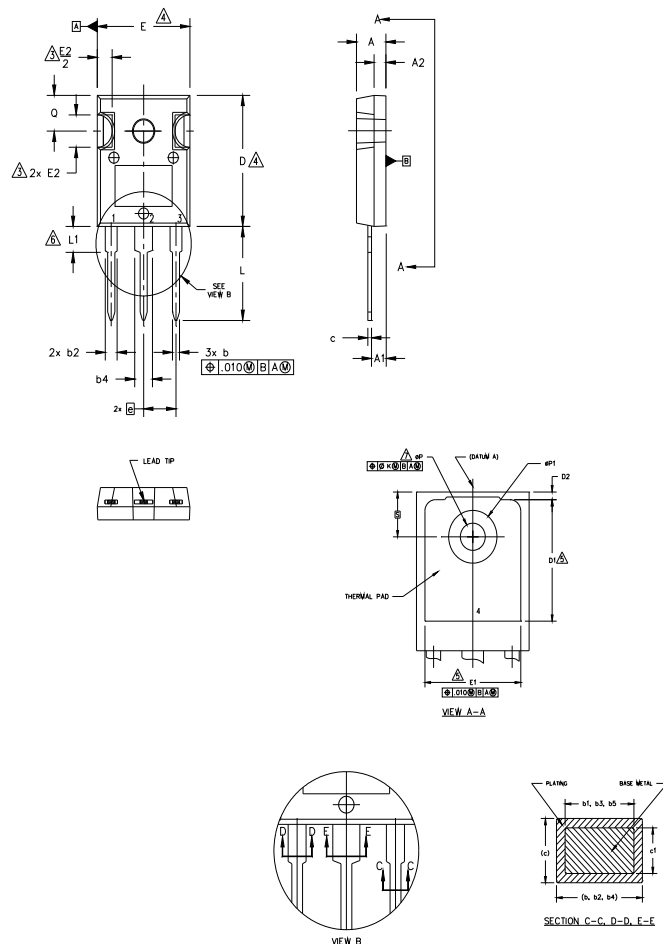


Fig. WF2 - Typ. Turn-on Loss Waveform
@ $T_J = 175^\circ\text{C}$ using Fig. CT.3

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	—	13.08	—	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	—	13.46	—	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	—	.291	—	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

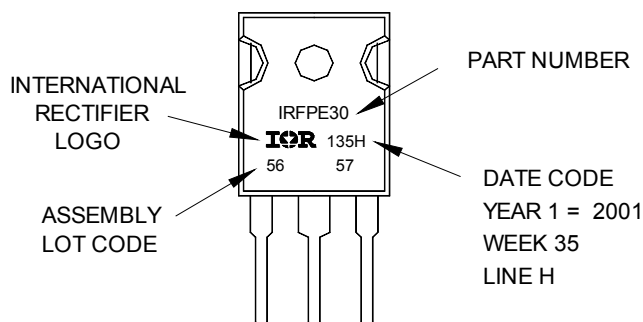
- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"

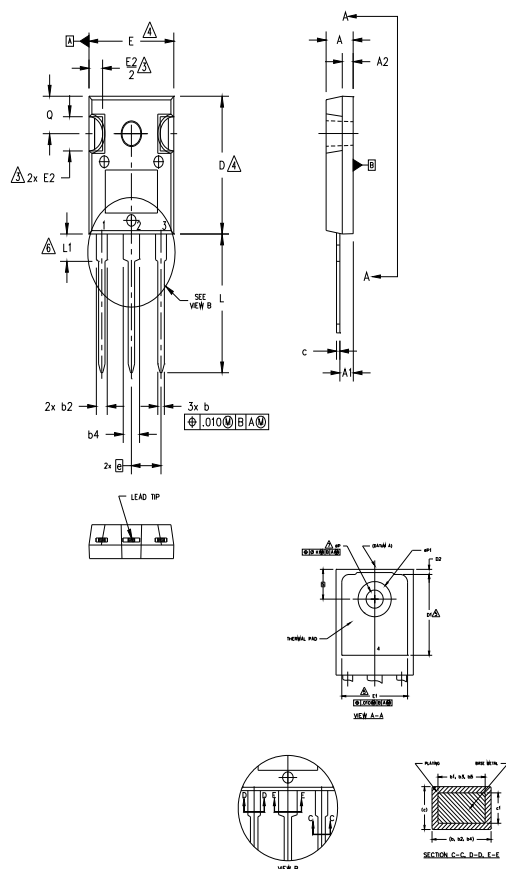


TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
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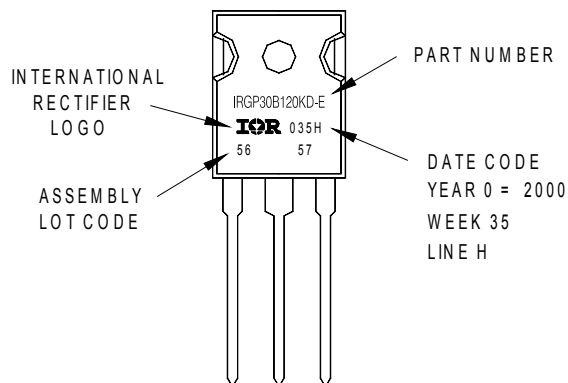
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial	
Moisture Sensitivity Level	TO-247AC	N/A
	TO-247AD	
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>