Silicon PNP Power Transistors 2N4898 2N4899 2N4900

DESCRIPTION

- ·· With TO-66 package
- Low collector-emitter saturation voltage
- Excellent safe operating area
- 2N4900 complement to type 2N4912

APPLICATIONS

- Designed for driver circuits,switching and amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Fig.1 simplified outline (TO-66) and symbol

Absolute maximum ratings(Ta=℃)

SYMBOL	PARAMETER		CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	2N4898	Open emitter	40	V
		2N4899		60	
		2N4900		80	
V_{CEO}	Collector-emitter voltage	2N4898	Open base	40	V
		2N4899		60	
		2N4900		80	
V_{EBO}	Emitter-base voltage		Open collector	5	V
I_C	Collector current			1.0	A
I_{CM}	Collector current-peak			4.0	A
I_B	Base current			1.0	A
P_D	Total Power Dissipation		T_C=25℃	25	W
T_j	Junction temperature			150	℃
T_{stg}	Storage temperature			-65~200	℃

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	Thermal resistance junction to case	7.0	℃/W

CHARACTERISTICS

Tj=25℃ unless otherwise specified

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(sus)}$	Collector-emitter sustaining voltage	2N4898	I_C=0.1A ;I_B=0	40			V
		2N4899		60			
		2N4900		80			
V_{CEsat}	Collector-emitter saturation voltage		I_C=1A; I_B=0.1A			0.6	V
V_{BEsat}	Collector-emitter saturation voltage		I_C=1A ;I_B=0.1A			1.3	V
V_{BE}	Base-emitter on voltage		I_C=1A ; V_{CE}=1V			1.3	V
I_{CEO}	Collector cut-off current	2N4898	V_{CE}=20V; I_B=0			0.5	mA
		2N4899	V_{CE}=30V; I_B=0				
		2N4900	V_{CE}=40V; I_B=0				
I_{CEX}	Collector cut-off current		V_{CE}=Rated V_{CEO}; $V_{BE(off)}$=1.5V T_C=150℃			0.1 1.0	mA
I_{CBO}	Collector cut-off current		V_{CB}=Rated V_{CBO}; I_E=0			0.1	mA
I_{EBO}	Emitter cut-off current		V_{EB}=5V; I_C=0			1.0	mA
h_{FE-1}	DC current gain		I_C=50mA ; V_{CE}=1V	40			
h_{FE-2}	DC current gain		I_C=500mA ; V_{CE}=1V	20		100	
h_{FE-3}	DC current gain		I_C=1.0A ; V_{CE}=1V	10			
C_{OB}	Output capacitance		I_E=0;V_{CB}=10V;f=1MHz			100	pF
f_T	Transition frequency		I_C=250mA;V_{CE}=10V	3.0			MHz

PACKAGE OUTLINE

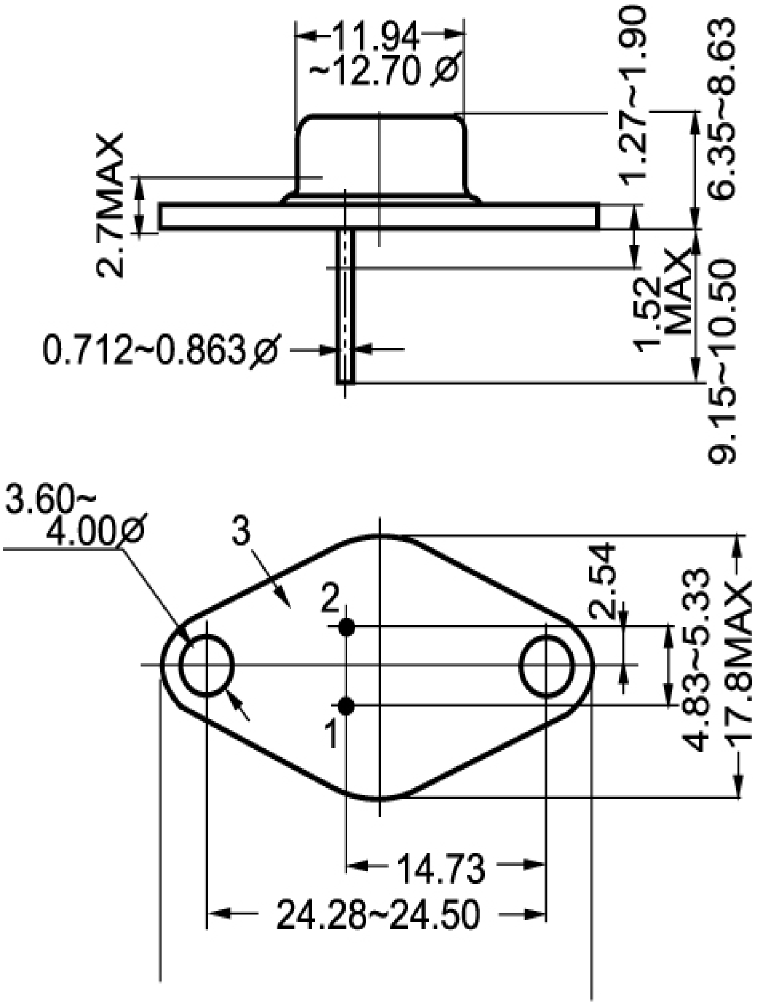

Fig.2 outline dimensions