

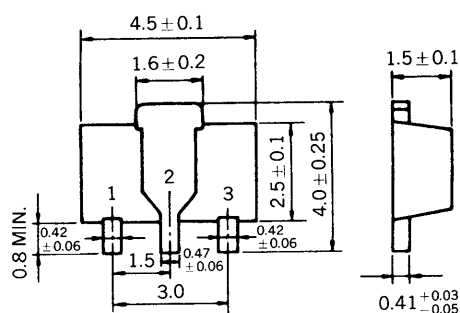
MOS FIELD EFFECT TRANSISTOR

2SJ212

P-CHANNEL MOS FET

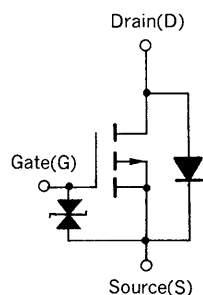
FOR SWITCHING

PACKAGE DIMENSIONS (Unit : mm)



1. Source
2. Drain
3. Gate

MARK : PO



(Diode in the figure is the parasitic diode.)

The 2SJ212, P-channel vertical type MOS FET, is a switching device which can be driven directly by the output of ICs having a 5 V power source.

As the MOS FET has low on-state resistance and excellent switching characteristics, it is suitable for driving actuators such as motors, relays, and solenoids.

FEATURES

- Directly driven by ICs having a 5 V power supply.

- Has low on-state resistance

$$R_{DS(on)} = 4.0 \, \Omega \text{ MAX. @ } V_{GS} = -4.0 \text{ V, } I_D = -0.3 \text{ A}$$

$$R_{DS(on)} = 3.0 \, \Omega \text{ MAX. @ } V_{GS} = -10 \text{ V, } I_D = -0.3 \text{ A}$$

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

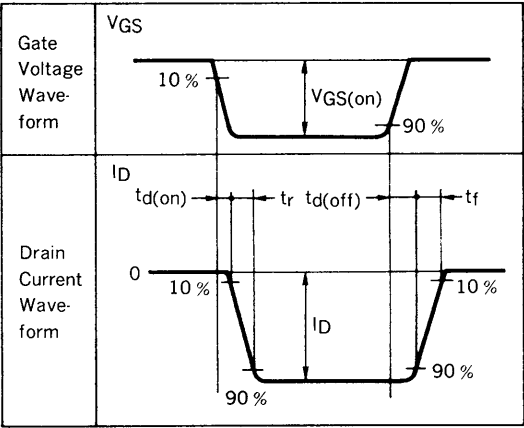
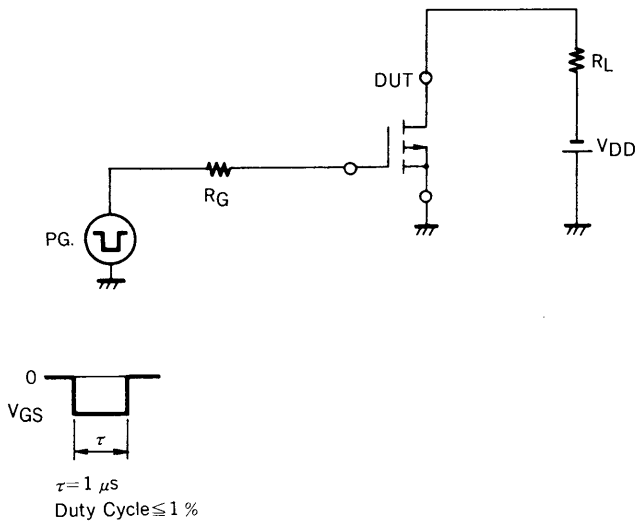
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

PARAMETER	SYMBOL	RATINGS	UNIT	TEST CONDITIONS
Drain to Source Voltage	V_{DSS}	-60	V	$V_{GS} = 0$
Gate to Source Voltage	V_{GSS}	± 20	V	$V_{DS} = 0$
Drain Current	$I_D(\text{DC})$	± 500	mA	
Drain Current	$I_D(\text{pulse})$	± 1.0	A	$PW \leq 10 \text{ ms, Duty Cycle} \geq 50 \%$
Total Power Dissipation	P_T	2.0	W	when using ceramic board of $16 \text{ cm}^2 \times 0.7 \text{ mm}$
Channel Temperature	T_{ch}	150	$^\circ\text{C}$	
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$	

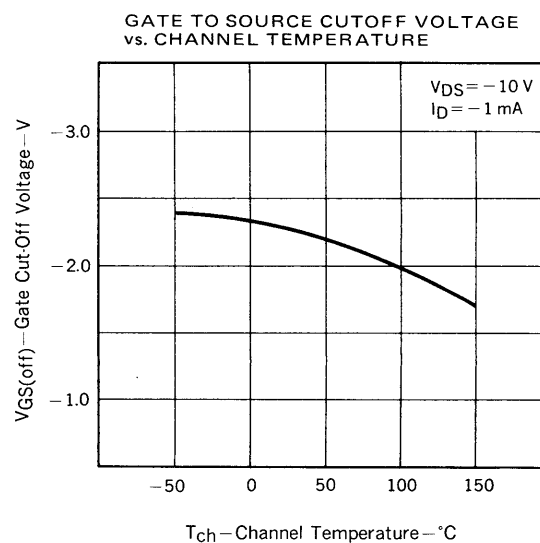
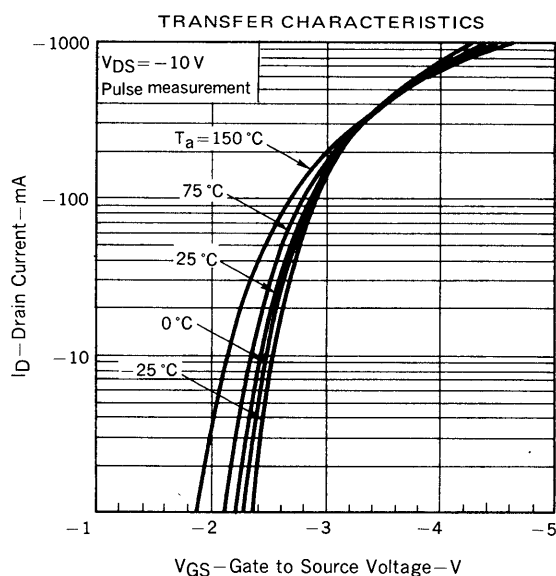
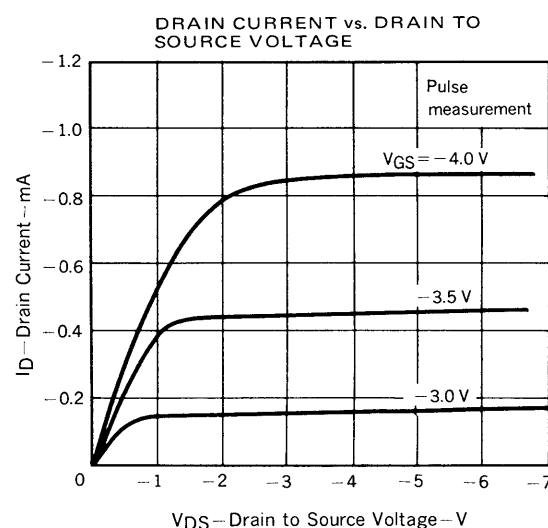
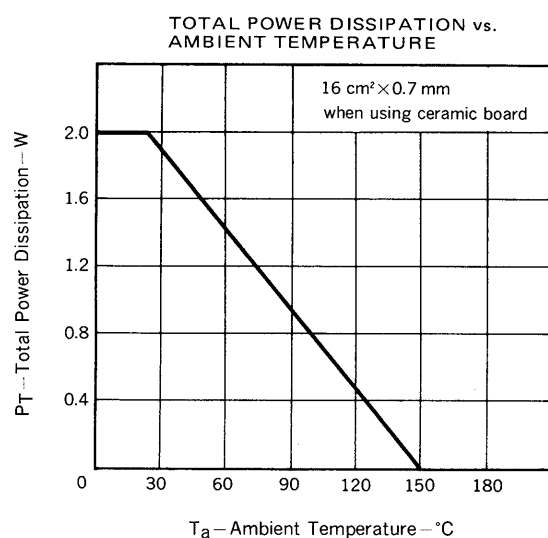
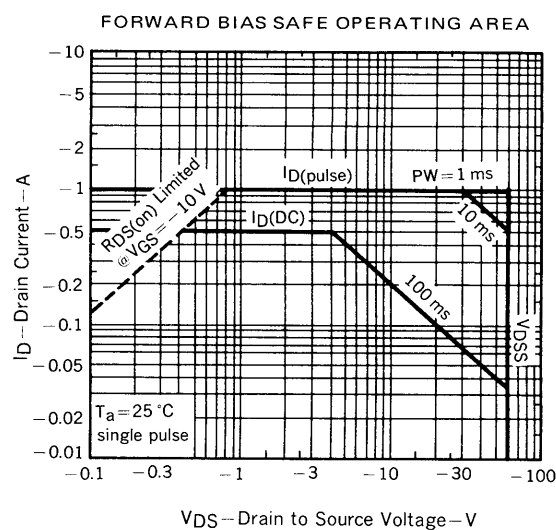
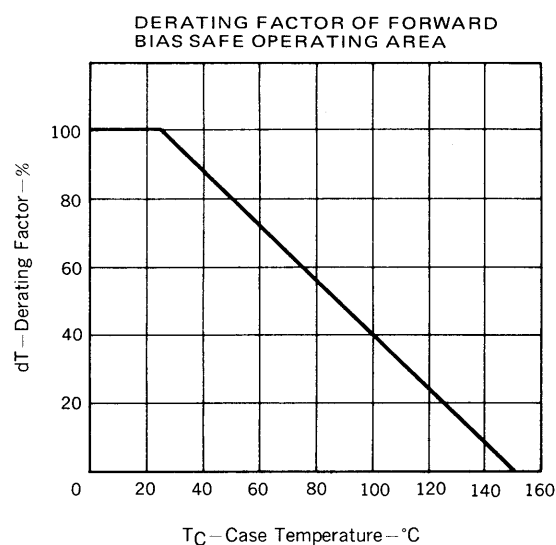
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Cut-off Current	I _{DSS}			−10	μA	V _{DS} = −60 V, V _{GS} = 0
Gate Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Gate Cut-off Voltage	V _{GS(off)}	−1.0	−2.2	−3.0	V	V _{DS} = −10 V, I _D = −1 mA
Forward Transfer Admittance	Y _{fs}	0.4	0.54		S	V _{DS} = −5 V, I _D = −0.3 A
Drain to Source On-State Resistance	R _{DS(on)1}		1.5	4.0	Ω	V _{GS} = −4.0 V, I _D = −0.3 A
Drain to Source On-State Resistance	R _{DS(on)2}		0.8	3.0	Ω	V _{GS} = −10 V, I _D = −0.5 A
Input Capacitance	C _{iss}		160		pF	V _{DS} = −5.0 V, V _{GS} = 0, f = 1 MHz
Output Capacitance	C _{oss}		100		pF	
Feedback Capacitance	C _{rss}		25		pF	
Turn-On Delay Time	t _{d(on)}		130		ns	V _{GS(on)} = −4 V, R _G = 10 Ω, V _{DD} = −5 V, I _D = −0.3 A, R _L = 1.5 Ω
Rise Time	t _r		380		ns	
Turn-Off Delay Time	t _{d(off)}		95		ns	
Fall Time	t _f		140		ns	

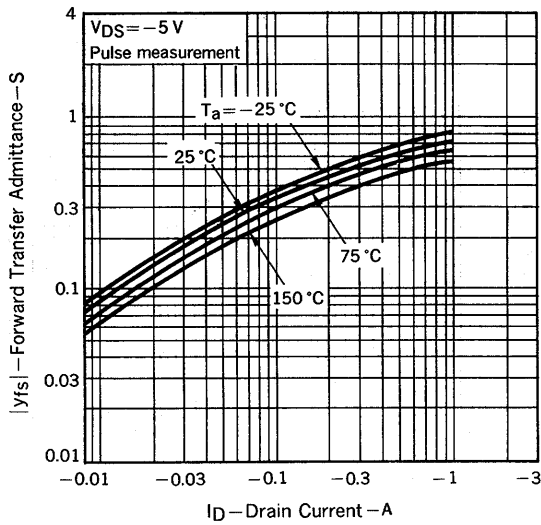
SWITCHING TIME MEASUREMENT CIRCUIT AND CONDITIONS



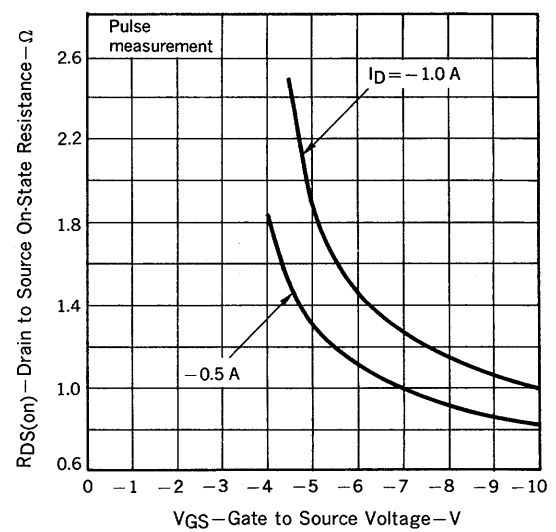
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



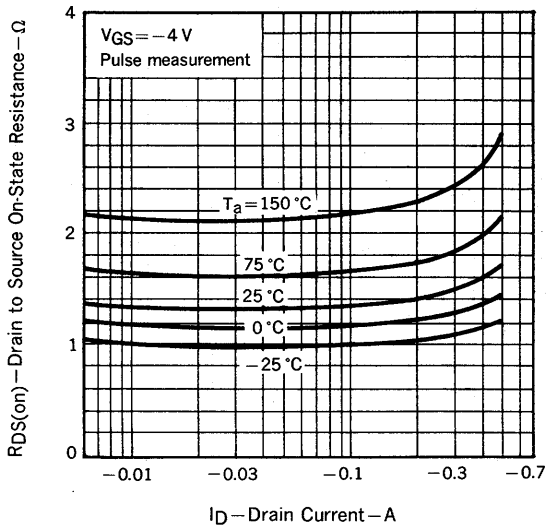
FORWARD TRANSFER ADMITTANCE
vs. DRAIN CURRENT



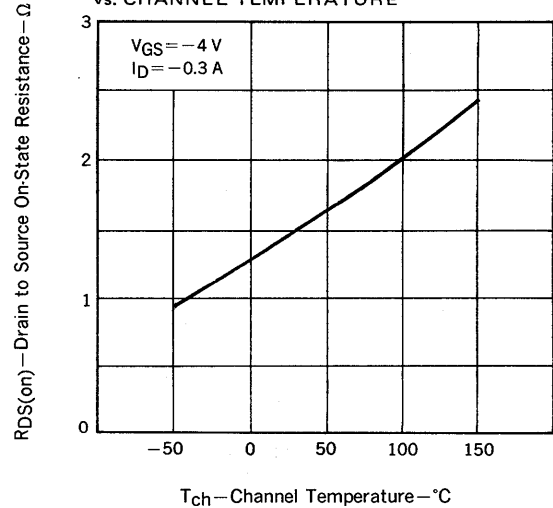
DRAIN TO SOURCE ON-STATE RESISTANCE
vs. GATE TO SOURCE VOLTAGE



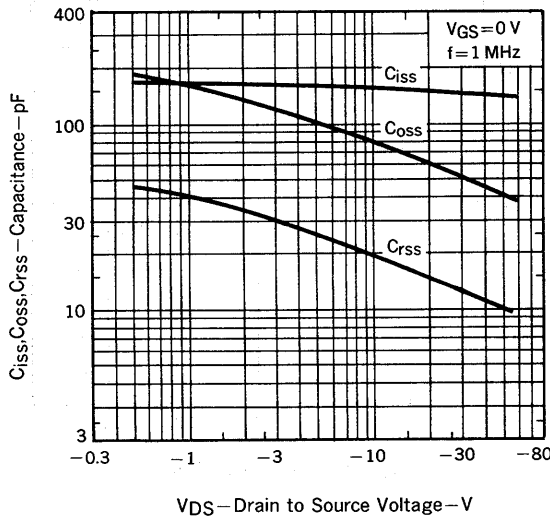
DRAIN TO SOURCE ON-STATE RESISTANCE
vs. DRAIN CURRENT



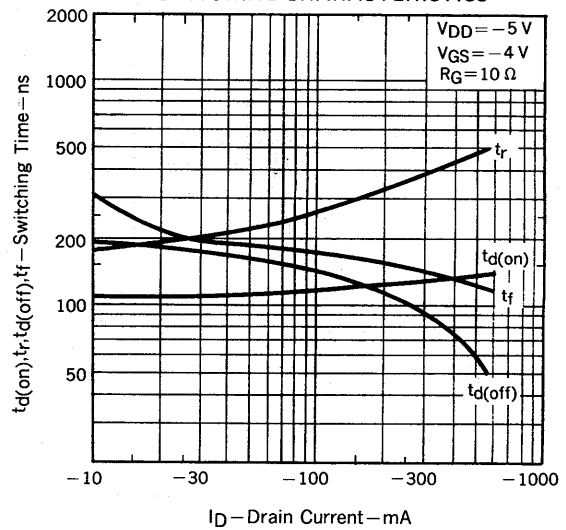
DRAIN TO SOURCE ON-STATE RESISTANCE
vs. CHANNEL TEMPERATURE

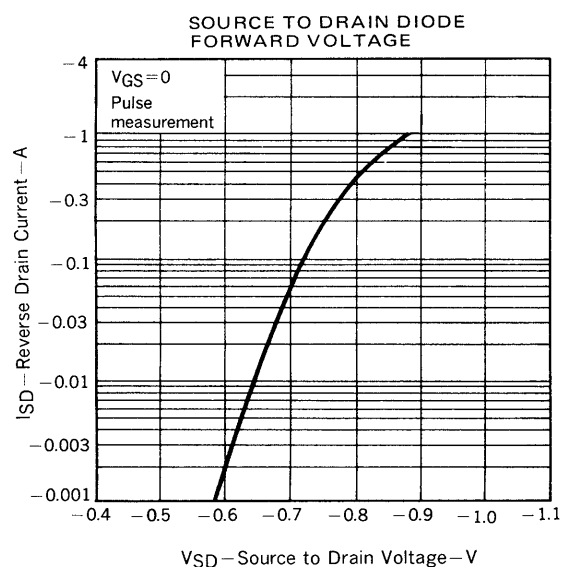


CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE



SWITCHING CHARACTERISTICS





RECOMMENDED SOLDERING CONDITIONS

Mounting of this product by soldering should be done under the following conditions.

Please consult our representatives about soldering methods and conditions other than these.

SURFACE MOUNT TYPE

For details of the recommended soldering conditions, see the information document.

"Device Mounting Manual for Surface Mounting (IEI-1207)."

Soldering Method	Soldering Conditions	Symbol for Recommended Conditions
Infrared Reflow	Package peak temp.: 230 °C Soldering time: within 30 sec (above 210 °C) Soldering times: 1, Days limitation: none*	IR30-00
Vapor Phase Soldering	Package peak temp.: 215 °C Soldering time: within 40 sec (above 200 °C) Soldering times: 1, Days limitation: none*	VP15-00
Wave Soldering	Soldering bath temp.: below 260 °C Soldering time: within 10 sec Soldering times: 1, Days limitation: none*	WS60-00

*: Stored days under storage conditions at 25 °C and below 65 % R.H. after the dry-pack has been opened.

Note 1 Combination of soldering methods should be avoided.

REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134

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Application examples recommended by NEC Corporation

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.