

P-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

2SJ330

SWITCHING

P-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SJ330 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 40 \text{ m}\Omega \text{ TYP. (} V_{GS} = -10 \text{ V, } I_D = -10 \text{ A)}$
 $R_{DS(on)} = 70 \text{ m}\Omega \text{ TYP. (} V_{GS} = -4 \text{ V, } I_D = -8 \text{ A)}$
- Low C_{iss} $C_{iss} = 2570 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

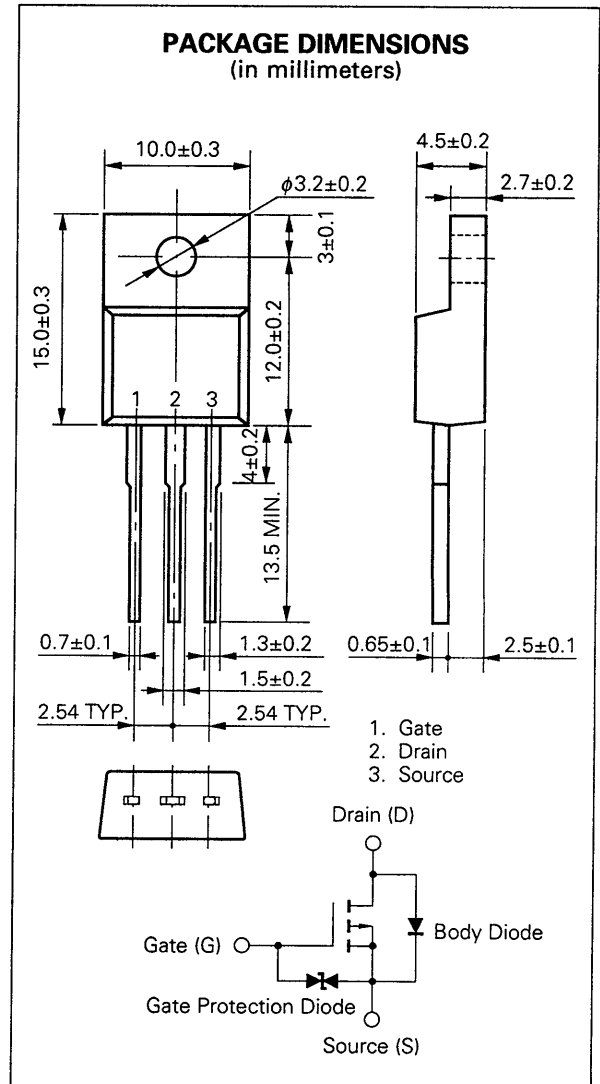
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	-60	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Gate to Source Voltage	$V_{GSS(DC)}$	-20, +10	V
Drain Current (DC)	$I_D(DC)$	± 20	A
Drain Current (pulse)	$I_D(pulse)^*$	± 80	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	35	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C MAX.}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

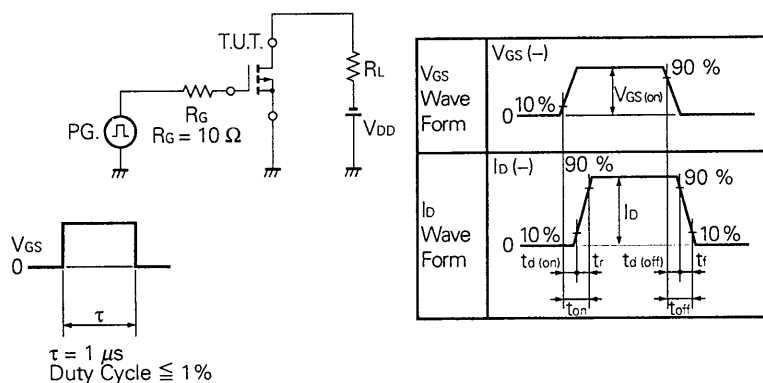
PACKAGE DIMENSIONS (in millimeters)



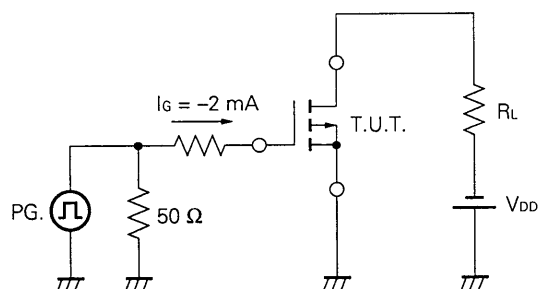
ELECTRICAL CHARACTERISTICS ($T_a = 25\text{ }^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.04	0.05	Ω	$V_{GS} = -10\text{ V}$, $I_D = -10\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)}$		0.07	0.09	Ω	$V_{GS} = -4\text{ V}$, $I_D = -8\text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	-1.0	-1.6	-2.0	V	$V_{DS} = -10\text{ V}$, $I_D = -1\text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	10			S	$V_{DS} = -10\text{ V}$, $I_D = -10\text{ A}$
Drain Leakage Current	I_{DSS}			-10	μA	$V_{DS} = -60\text{ V}$, $V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 10	μA	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0$
Input Capacitance	C_{iss}		2 570		pF	$V_{DS} = -10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$
Output Capacitance	C_{oss}		1 460		pF	
Reverse Transfer Capacitance	C_{rss}		640		pF	
Turn-On Delay Time	$t_{d(on)}$		50		ns	$V_{GS(on)} = -10\text{ V}$ $V_{DD} = -30\text{ V}$ $I_D = -10\text{ A}$, $R_G = 10\text{ }\Omega$ $R_L = 3.0\text{ }\Omega$
Rise Time	t_r		200		ns	
Turn-Off Delay Time	$t_{d(off)}$		340		ns	
Fall Time	t_f		230		ns	
Total Gate Charge	Q_G		90		nC	$V_{GS} = -10\text{ V}$ $I_D = -20\text{ A}$ $V_{DD} = -48\text{ V}$
Gate to Source Charge	Q_{GS}		7		nC	
Gate to Drain Charge	Q_{GD}		36		nC	
Diode Forward Voltage	V_{SD}		0.9		V	$I_F = 20\text{ A}$, $V_{GS} = 0$
Reverse Recovery Time	t_{rr}		100		ns	$I_F = 20\text{ A}$, $V_{GS} = 0$ $di/dt = 50\text{ A}/\mu\text{s}$
Reverse Recovery Charge	Q_{rr}		490		nC	

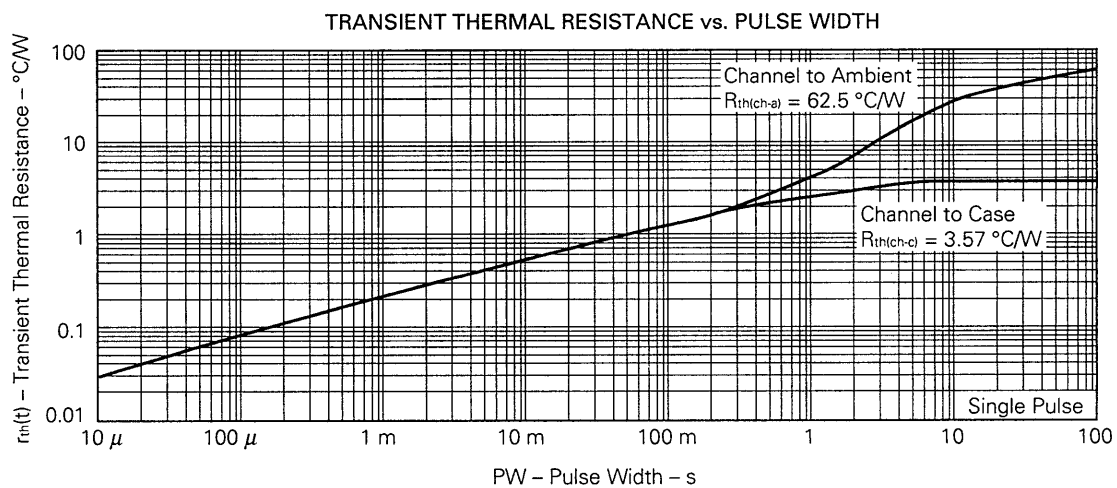
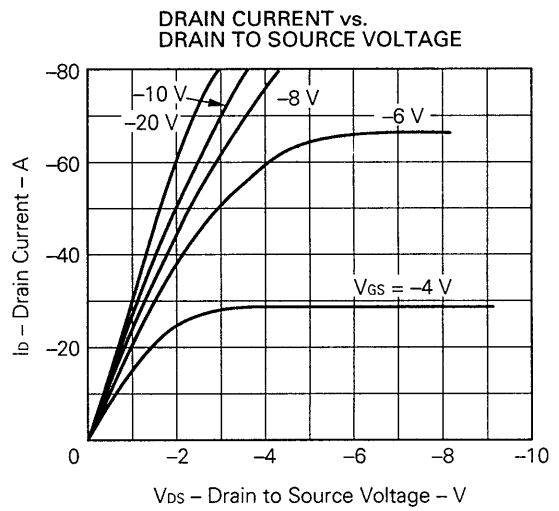
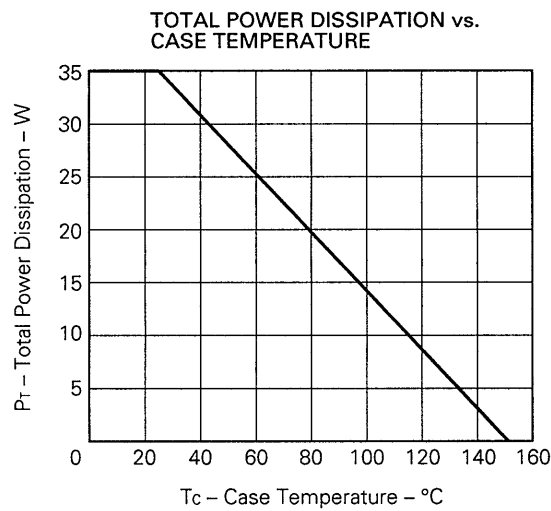
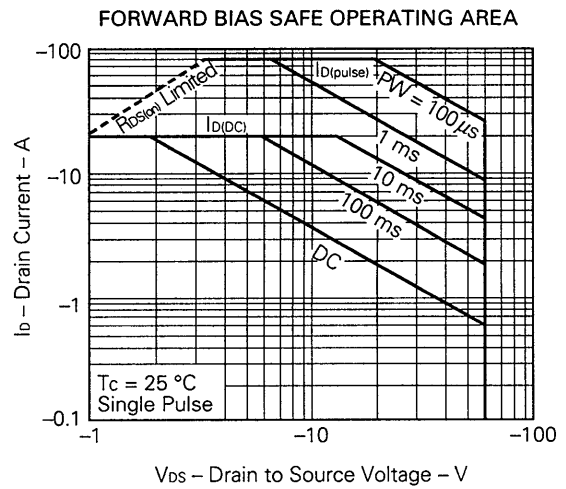
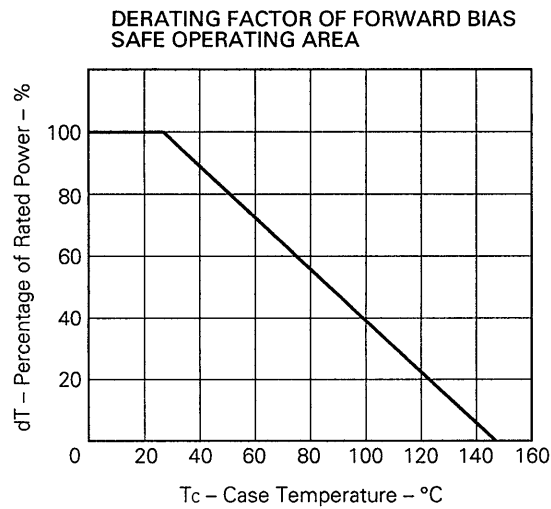
Test Circuit 1: Switching Time



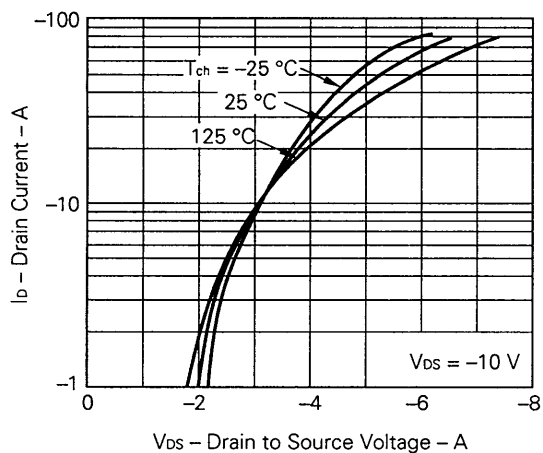
Test Circuit 2: Gate Charge



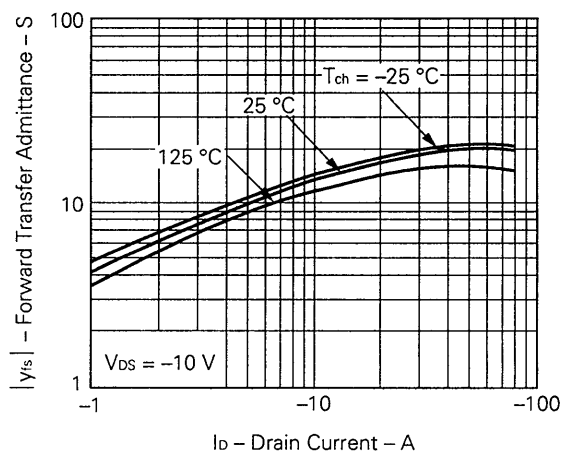
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



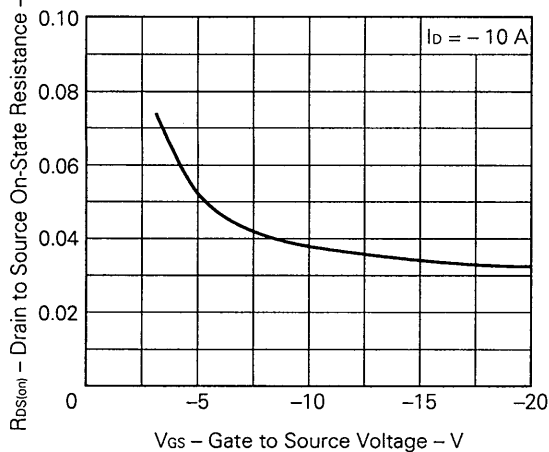
TRANSFER CHARACTERISTICS



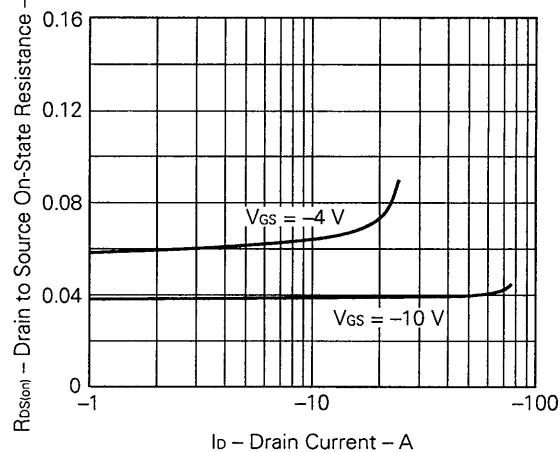
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



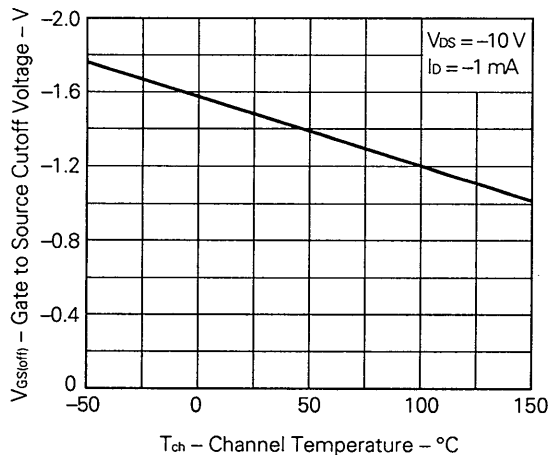
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



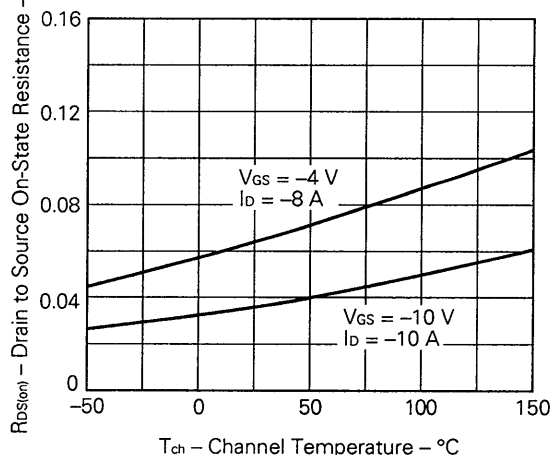
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



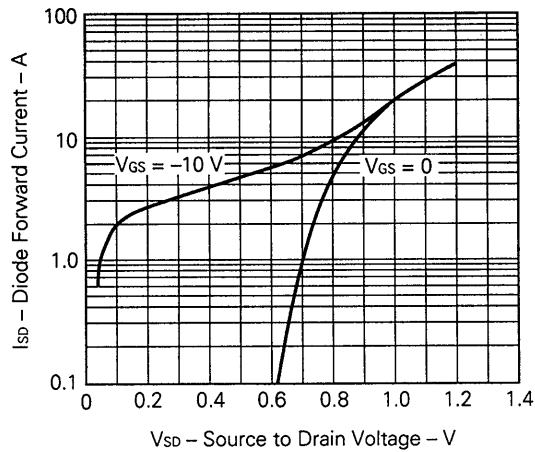
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



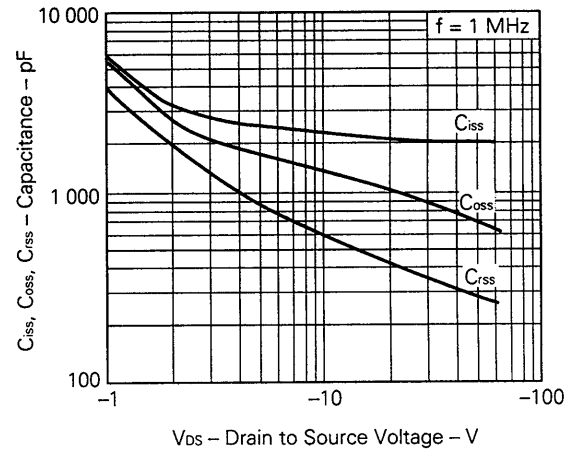
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



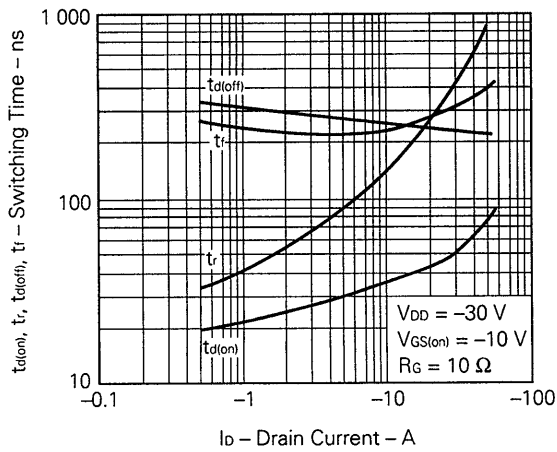
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



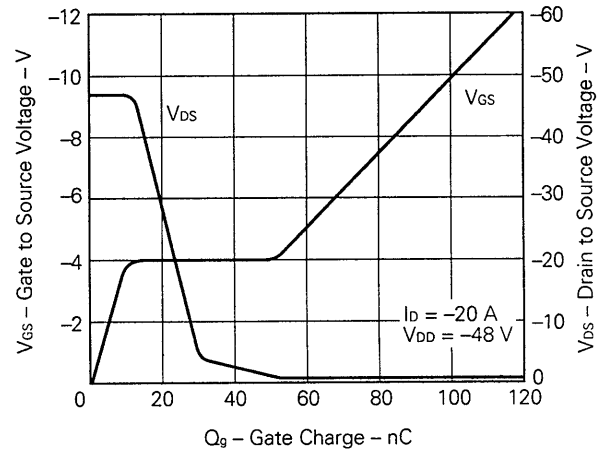
CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE



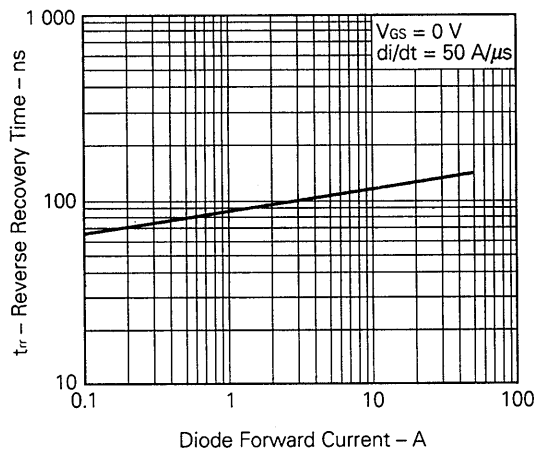
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs.
REVERSE DRAIN CURRENT



Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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