

N-Channel Power MOSFET 14A, 500Volts

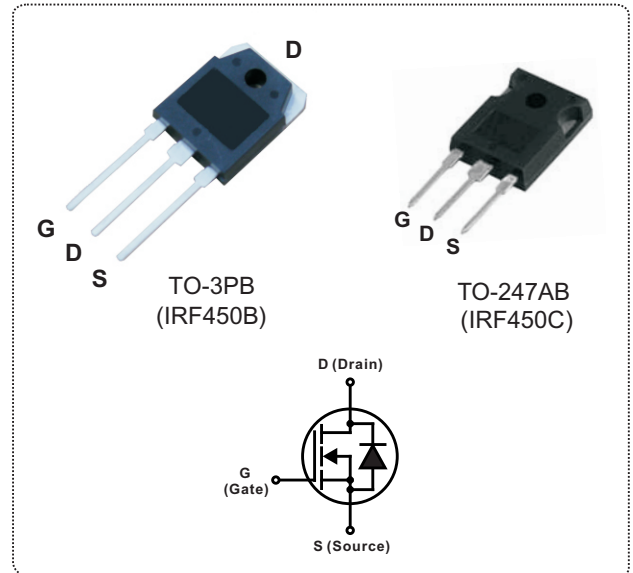
DESCRIPTION

The Nell **IRF450** is a three-terminal silicon device with current conduction capability of 14A, fast switching speed, low on-state resistance, breakdown voltage rating of 500V, and max. threshold voltage of 4 volts.

They are designed for use in applications such as switched mode power supplies, DC to DC converters, motor control, circuits UPS and general purpose switching applications.

FEATURES

- $R_{DS(ON)} = 0.40\Omega$ @ $V_{GS} = 10V$
- Ultra low gate charge(150nC Max.)
- Low reverse transfer capacitance ($C_{RSS} = 340pF$ typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature



PRODUCT SUMMARY

I_D (A)	14
V_{DSS} (V)	500
$R_{DS(ON)}$ (Ω)	0.40 @ $V_{GS} = 10V$
Q_G (nC) max.	150

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ unless otherwise specified)

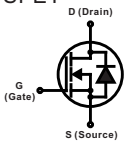
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltage	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	Drain to Gate voltage	$R_{GS} = 20K\Omega$	500	
V_{GS}	Gate to Source voltage		± 20	
I_D	Continuous Drain Current ($V_{GS} = 10V$)	$T_C = 25^\circ C$	14	A
		$T_C = 100^\circ C$	8.7	
I_{DM}	Pulsed Drain current(Note 1)		56	
I_{AR}	Avalanche current(Note 1)		8.7	mJ
E_{AR}	Repetitive avalanche energy(Note 1)	$I_{AR} = 14A, R_{GS} = 50\Omega, V_{GS} = 10V$	19	
E_{AS}	Single pulse avalanche energy(Note 2)	$I_{AS} = 14A, L = 7.0mH$	760	
dv/dt	Peak diode recovery dv/dt(Note 3)		3.5	V /ns
P_D	Total power dissipation	$T_C = 25^\circ C$	190	W
	Derate above $25^\circ C$		1.5	W / $^\circ C$
T_J	Operation junction temperature		-55 to 150	$^\circ C$
T_{STG}	Storage temperature		-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N·m)

Note: 1. Repetitive rating: pulse width limited by junction temperature.
 2. $I_{AS} = 14A, L = 7.0mH, V_{DD} = 50V, R_G = 25\Omega$, starting $T_J = 25^\circ C$.
 3. $I_{SD} \leq 14A, di/dt \leq 130A/\mu s, V_{DD} \leq V_{(BR)DSS}$, starting $T_J = 25^\circ C$.

Nell High Power Products

THERMAL RESISTANCE						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	
$R_{th(j-c)}$	Thermal resistance, junction to case			0.65	°C/W	
$R_{th(c-s)}$	Thermal resistance, case to heat sink		0.24			
$R_{th(j-a)}$	Thermal resistance, junction to ambient			40		

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
◎ STATIC						
$V_{(BR)DSS}$	Drain to source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	500			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	$I_D = 1\text{mA}$, $V_{DS} = V_{GS}$		0.63		V/°C
I_{DSS}	Drain to source leakage current	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$, $T_C = 25^\circ\text{C}$			25.0	μA
		$V_{DS}=400\text{V}$, $V_{GS}=0\text{V}$, $T_C=125^\circ\text{C}$			250	
I_{GSS}	Gate to source forward leakage current	$V_{GS} = 20\text{V}$, $V_{DS} = 0\text{V}$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -20\text{V}$, $V_{DS} = 0\text{V}$			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	$I_D = 8.4\text{A}$, $V_{GS} = 10\text{V}$			0.40	Ω
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
g_{fs}	Forward transconductance	$V_{DS} = 50\text{V}$, $I_D = 8.4\text{A}$	9.3			S
◎ DYNAMIC						
C_{ISS}	Input capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		2600		pF
C_{OSS}	Output capacitance			720		
C_{RSS}	Reverse transfer capacitance			340		
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 250\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 14\text{A}$, $R_G = 6.2\Omega$, $R_D = 17\Omega$ (Note1,2)		17		ns
t_r	Rise time			47		
$t_{d(OFF)}$	Turn-off delay time			92		
t_f	Fall time			44		
Q_G	Total gate charge	$V_{DD} = 400\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 14\text{A}$, (Note1,2)			150	nC
Q_{GS}	Gate to source charge				20	
Q_{GD}	Gate to drain charge (Miller charge)				80	
L_D	Internal drain inductance	Between lead, 6mm(0.25") form package and center of die contact		5		nH
L_S	Internal source inductance			13		

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SD}	Diode forward voltage	$I_{SD} = 14\text{A}$, $V_{GS} = 0\text{V}$			1.4	V
I_S (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET			14	A
I_{SM}	Pulsed source current				56	
t_{rr}	Reverse recovery time	$I_{SD} = 14\text{A}$, $V_{GS} = 0\text{V}$, $dI_F/dt = 100\text{A}/\mu\text{s}$		540	810	ns
Q_{rr}	Reverse recovery charge			4.8	7.2	μC

Note: 1. Pulse test: Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature.

ORDERING INFORMATION SCHEME

	IRF	450	B
MOSFET series			
N-Channel, IRF series			
Current and Voltage rating, I_D & V_{DS}			
14A / 500V			
Package type			
B = TO-3PB			
C = TO-247AB			

■ TYPICAL CHARACTERISTICS

Fig.1 Typical output characteristics, $T_C=25^\circ\text{C}$

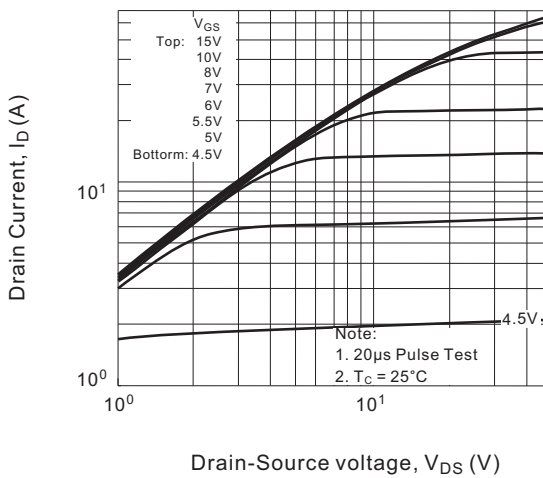


Fig.2 Typical transfer characteristics

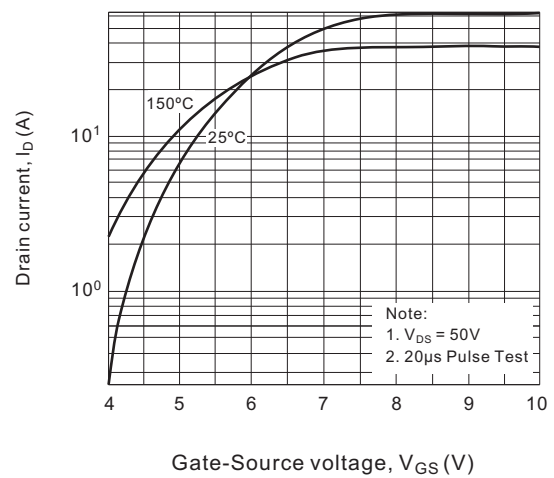


Fig.3 Typical output characteristics, $T_C=150^\circ\text{C}$

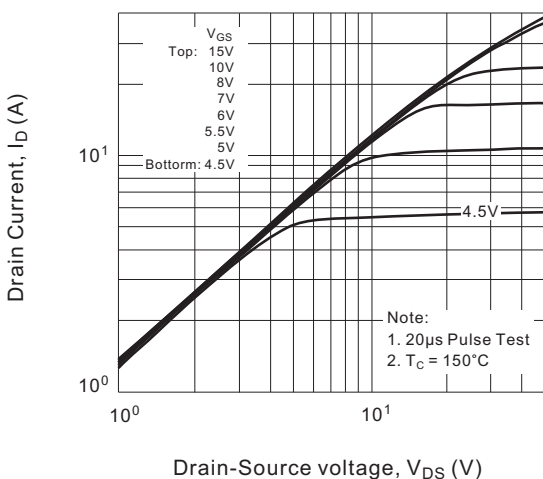


Fig.4 Normalized On-Resistance vs. Temperature

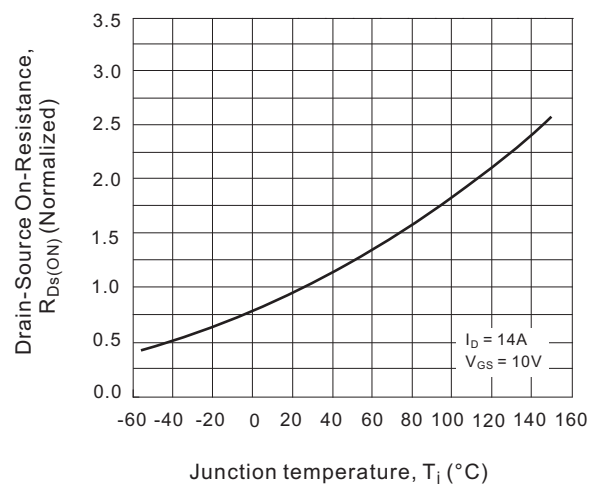


Fig.5 Typical capacitance vs. Drain-to-Source voltage

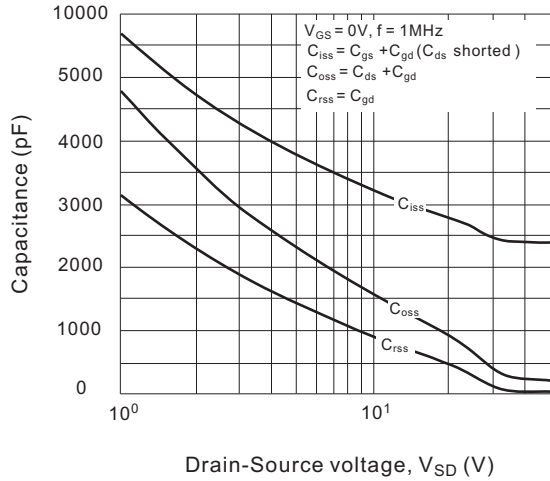


Fig.6 Typical source-drain diode forward voltage

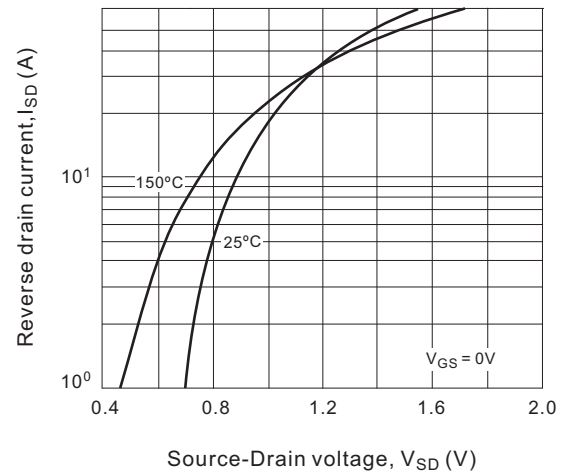


Fig.7 Typical gate charge vs. gate-to-source voltage

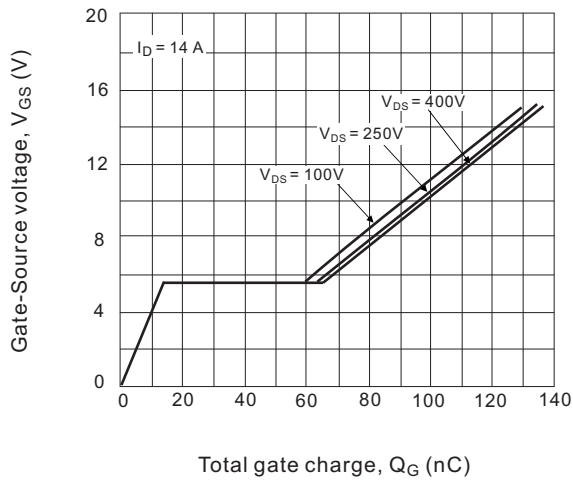


Fig.8 Maximum safe operating area

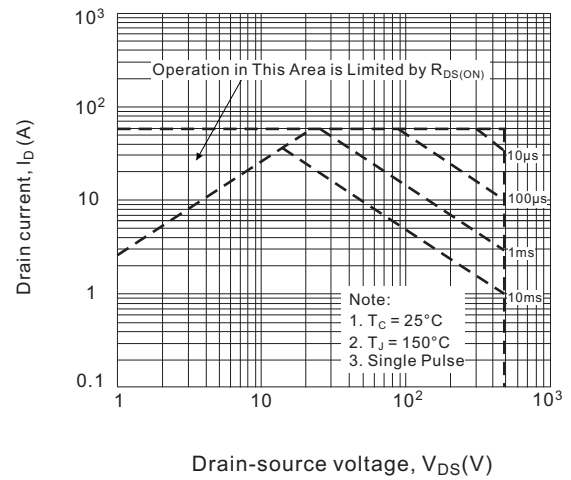


Fig.9 Maximum drain current vs. Case temperature

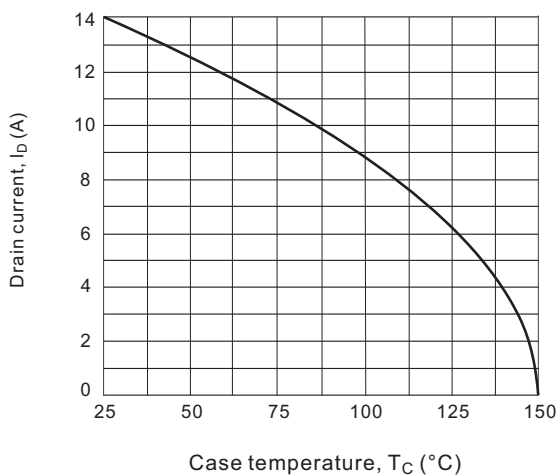


Fig.10 Maximum effective transient thermal impedance, Junction-to-Case

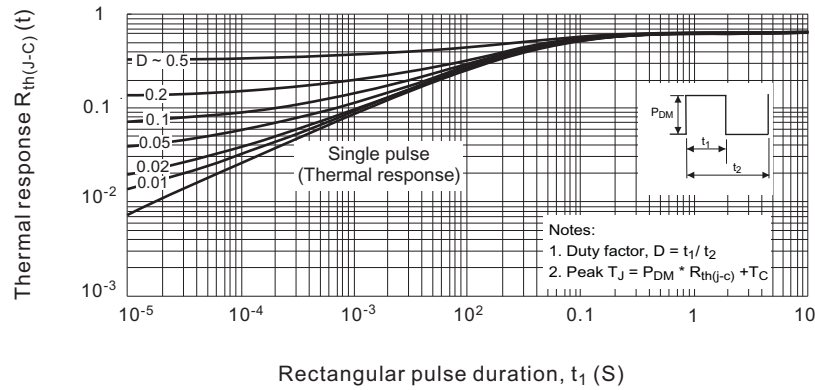


Fig.11a. Switching time test circuit

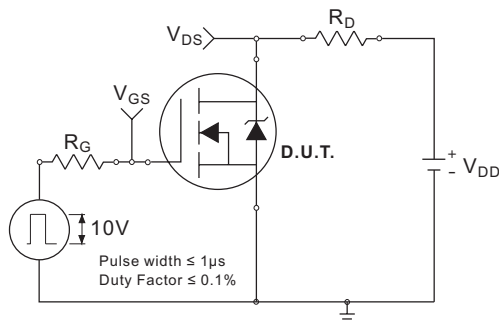


Fig.11b. Switching time waveforms

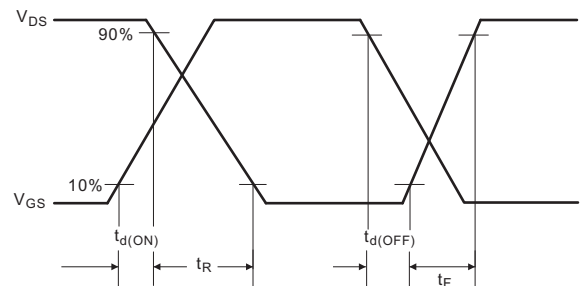


Fig.12a. Unclamped Inductive test circuit

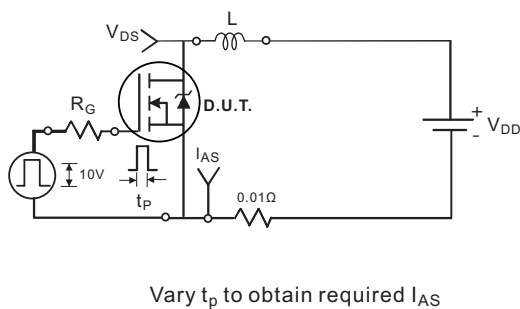


Fig.12b. Unclamped Inductive waveforms

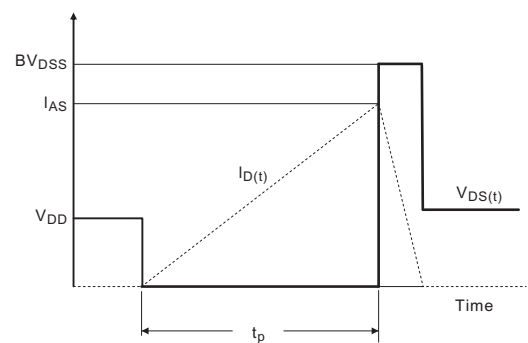


Fig.12c. Maximum avalanche energy vs. Drain current

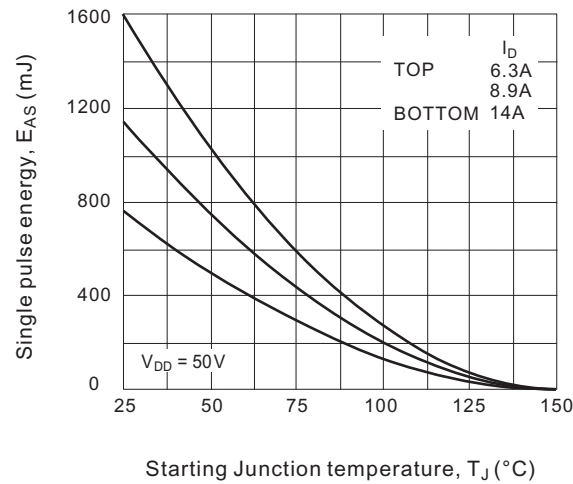


Fig.13a. Basic gate charge waveform

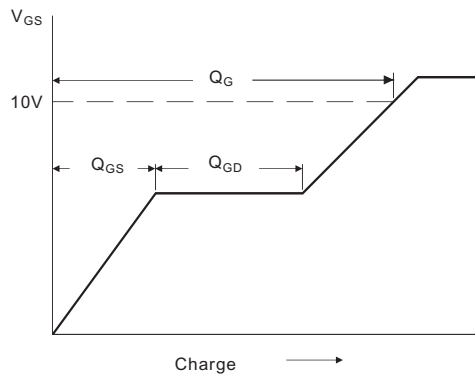


Fig.13b. Gate charge test circuit

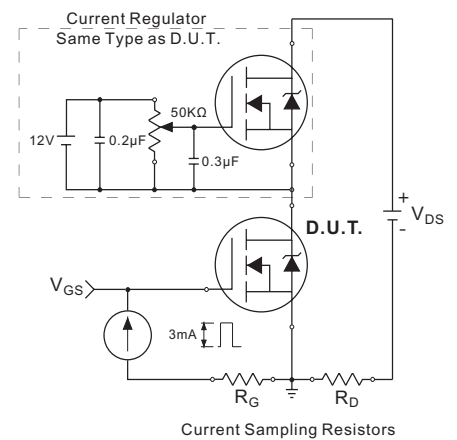
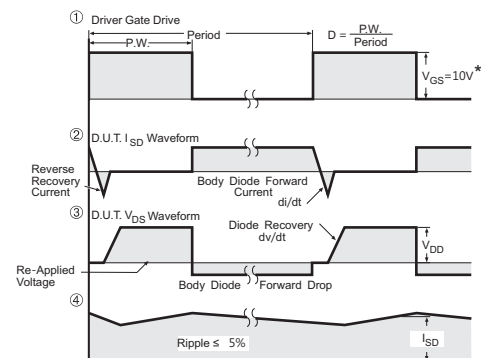
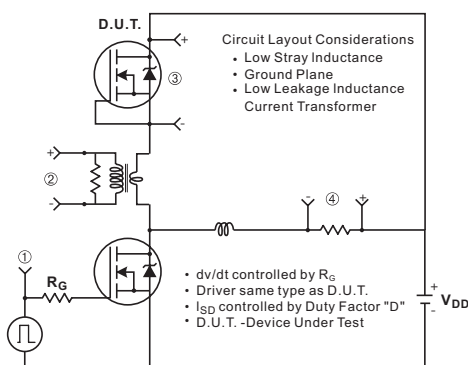
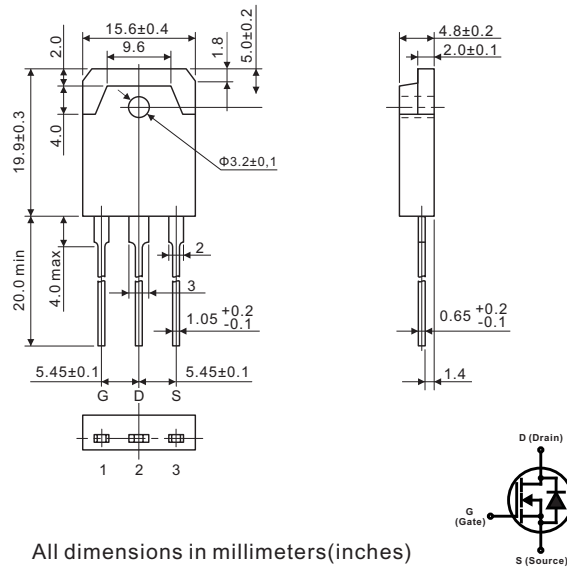


Fig.14 Peak diode recovery dv/dt test circuit for N-Channel MOSFET



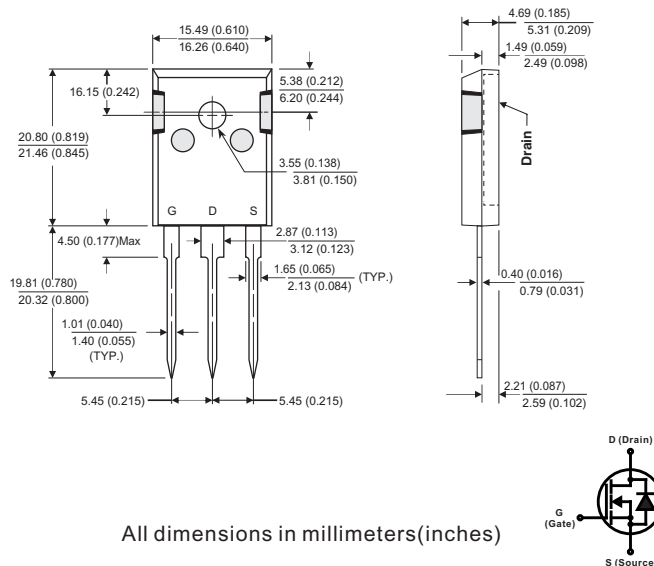
* $V_{GS} = 5V$ for Logic Level Devices and $3V$ for drive devices

TO-3PB



All dimensions in millimeters(inches)

TO-247AB



All dimensions in millimeters(inches)