

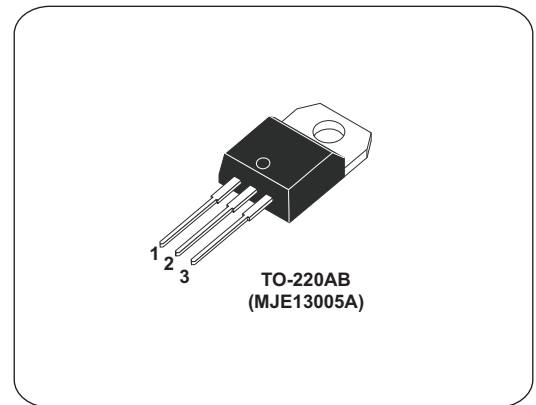
Switchmode Series NPN Silicon Power Transistors (4A / 400V / 75W)

FEATURES

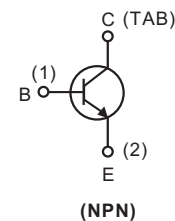
- $V_{CEO(SUS)} \geq 400V$ @ $I_C = 10\text{ mA}$, $I_B = 0$
- $V_{CE(sat)} = 1.0V$ (Max.) @ $I_C = 4\text{ A}$, $I_B = 1\text{ A}$
- Switching time - $t_f = 0.9\text{ }\mu s$ (Max.) @ $I_C = 2\text{ A}$
- 700V blocking capability

DESCRIPTION

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220V SWITCHMODE applications such as switching regulators, inverters, motor controls, solenoid/relay drivers and deflection circuits.



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ C$ unless otherwise specified)

SYMBOL	PARAMETER		VALUE	UNIT
V_{CEV}	Collector to base voltage ($V_{BE} = 0$)		700	V
V_{CEO}	Collector to emitter voltage ($I_B = 0$)		400	
V_{EBO}	Emitter to base voltage		9	
I_C	Collector current - continuous		4	A
I_{CM}	Peak collector current (Note 1)		8	
I_B	Base current - continuous		2	
I_{BM}	Peak base current (Note 1)		4	
I_E	Emitter current - continuous		6	
I_{EM}	Peak emitter current (Note 1)		12	
P_D	Total power dissipation	$T_C = 25^\circ C$	75	W
	Derate above $25^\circ C$		0.6	W/ $^\circ C$
T_j	Junction temperature		150	$^\circ C$
T_{stg}	Storage temperature		-65 to 150	
T_L	Maximum lead temperature for soldering purposes: 1/16" from case for ≤ 10 seconds		265	$^\circ C$

Note: 1. Pulse test : Pulse width = 5ms, duty cycle $\leq 10\%$

THERMAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)			
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-c)}$	Maximum thermal resistance, junction to case	1.67	$^\circ\text{C/W}$
$R_{th(j-a)}$	Maximum thermal resistance, junction to ambient	62.5.	

ELECTRICAL CHARACTERISTICS (T _C = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
◎ OFF CHARACTERISTICS						
I _{CEV}	Collector cutoff current	V _{CE} = 700V, V _{BE(off)} = 1.5V			1.0	mA
		V _{CE} = 700V, V _{BE(off)} = 1.5V, T _C = 100°C			5.0	
I _{CEO}	Collector cutoff current	V _{CE} = 400V, I _B = 0			0.1	
I _{EBO}	Emitter cutoff current	V _{EBO} = 9V, I _C = 0			1.0	
V _{CEO(SUS)} *	Collector to emitter sustaining voltage	I _C = 10mA, I _B = 0	400			V
V _{(BR)CEV}	Collector to base breakdown voltage	I _C = 10mA, V _{BE} = 0	700			
V _{(BR)EBO}	Emitter to base breakdown voltage	I _E = 10mA, I _C = 0	9			
◎ ON CHARACTERISTICS						
h _{FE}	Forward current transfer ratio (DC current gain)	I _C = 1A, V _{CE} = 5V	10		60	
		I _C = 2A, V _{CE} = 5V	8		40	
V _{CE(sat)} *	Collector to emitter saturation voltage	I _C = 1A, I _B = 0.2A			0.5	V
		I _C = 2A, I _B = 0.5A			0.6	
		I _C = 4A, I _B = 1A			1.0	
		I _C = 2A, I _B = 0.5A, T _C = 100°C			1.0	
V _{BE(on)} *	Base to emitter on voltage	I _C = 1A, I _B = 0.2A			1.2	V
		I _C = 2A, I _B = 0.5A			1.6	
		I _C = 2A, I _B = 0.5A, T _C = 100°C			1.5	
◎ DYNAMIC CHARACTERISTICS						
f _T	Transition frequency (Current gain- Bandwidth product)	I _C = 0.5A, V _{CE} = 10V, f _{test} = 1MHz	4			MHz
C _{ob}	Output capacitance	V _{CB} = 10V, I _E = 0, f _{test} = 0.1MHz		65		pF
◎ SWITCHING CHARACTERISTICS						
t _d	Delay time	V _{CC} = 125V, I _C = 2A I _{B1} = I _{B2} = 0.4A, t _p = 25μs duty clcye ≤1%		0.03	0.1	μs
t _r	Rise time			0.35	0.7	
t _s	Storage time			2.0	4.0	
t _f	Fall time			0.45	0.9	

*Pulsed : Pulse duration = 300 μs , duty cycle = 2%.

Fig.1 DC current gain

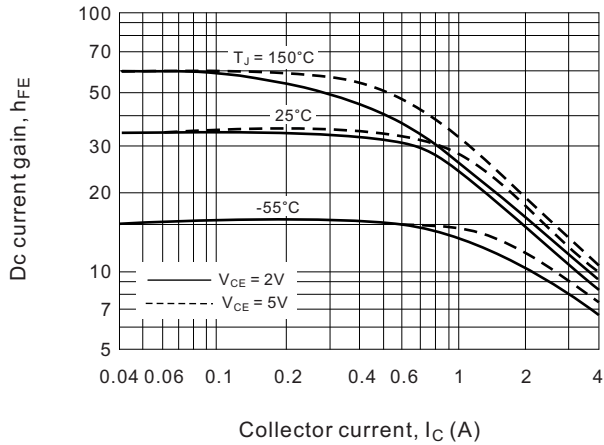


Fig.2 $V_{CE(sat)}$ - I_B characteristics (Typical)

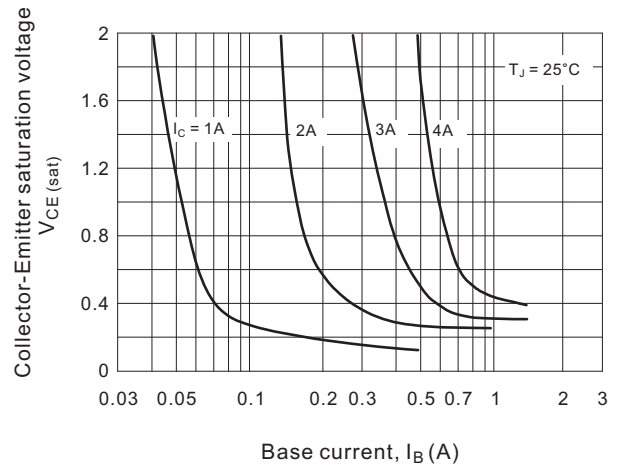


Fig.3 V_{BE} - I_C characteristics (Typical)

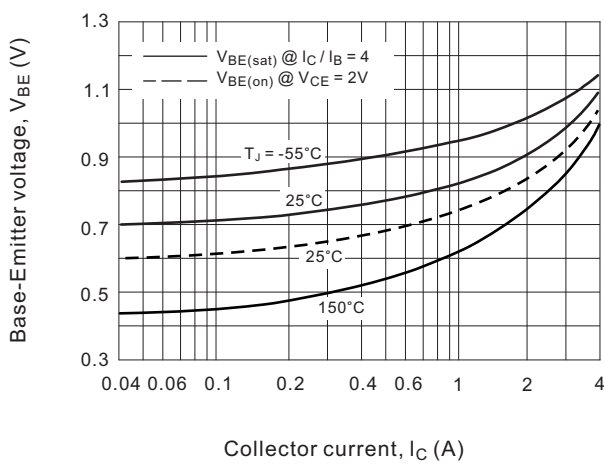


Fig.4 $V_{CE(sat)}$ - I_C characteristics (Typical)

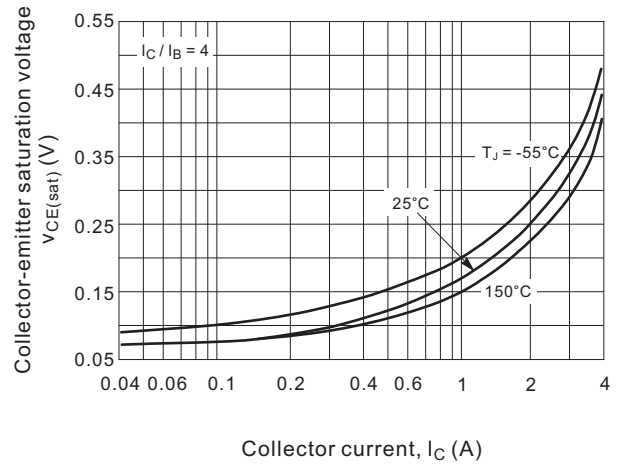


Fig.5 Collector cutoff region

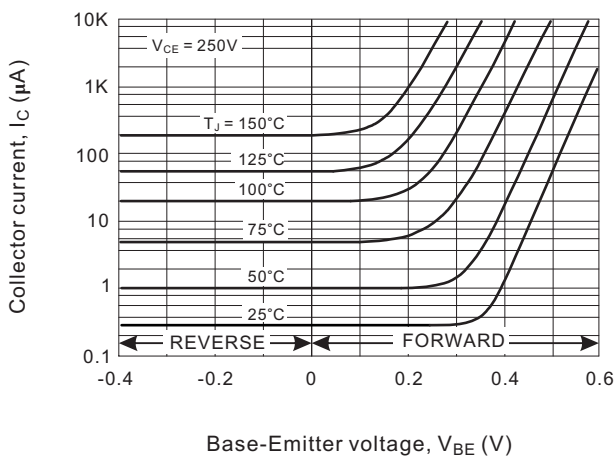


Fig.6 Capacitance

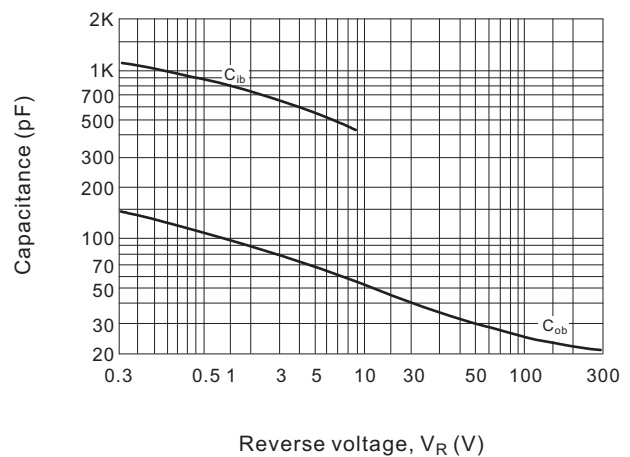
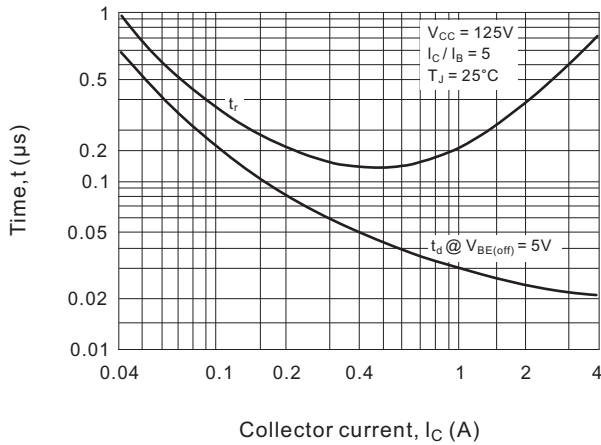
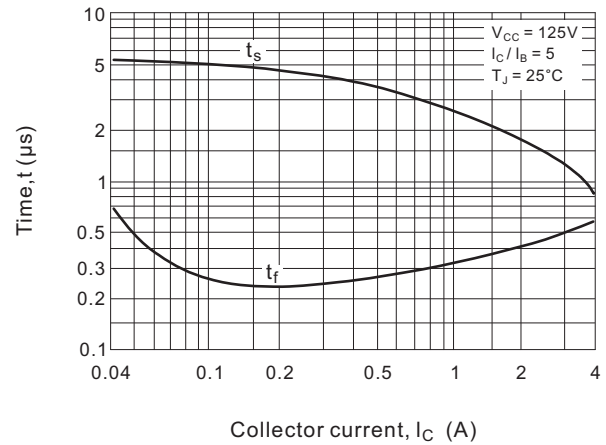


Fig.7 Turn-On time

Fig.8 Turn-Off time

Fig.9 Test conditions for dynamic performance

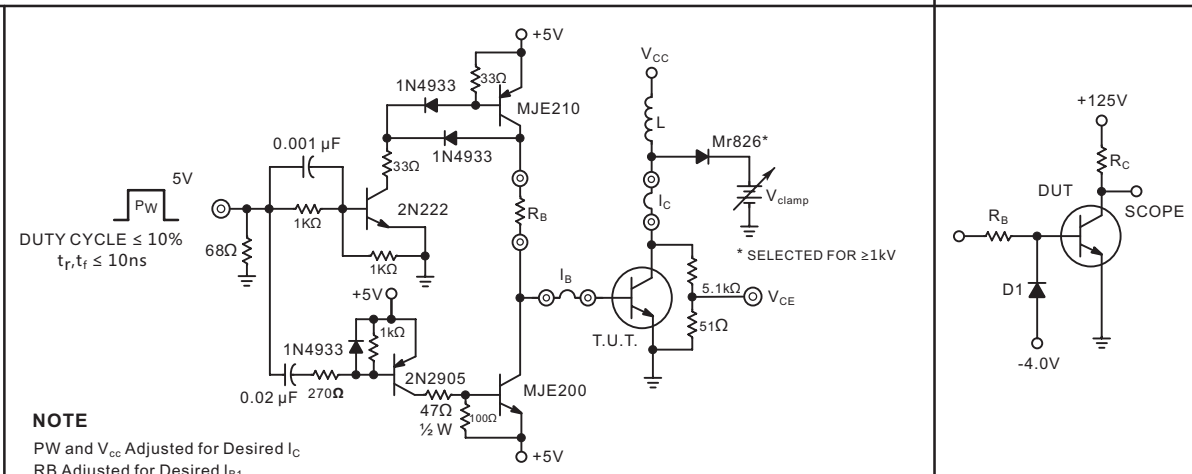
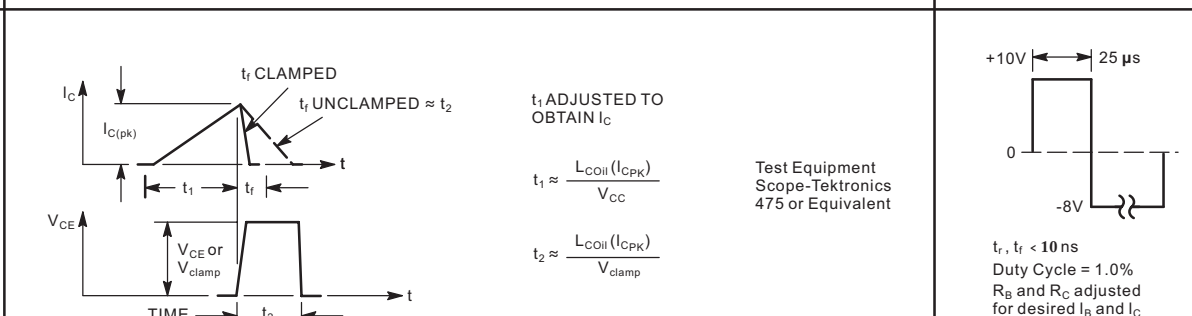
REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING			RESISTIVE SWITCHING
TEST CIRCUITS	 NOTE PW and V_{CC} Adjusted for Desired I_C RB Adjusted for Desired I_B		
CIRCUIT VALUES	Coil Data : Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 μH / 20A $L_{coil} = 200 \mu H$ $V_{CC} = 20V$ $V_{clamp} = 300 Vdc$		
TEST WAVEFORMS	 t_1 ADJUSTED TO OBTAIN I_C $t_1 \approx \frac{L_{COIL}(I_{CPK})}{V_{CC}}$ $t_2 \approx \frac{L_{COIL}(I_{CPK})}{V_{clamp}}$ Test Equipment Scope-Tektronics 475 or Equivalent $t_r, t_f < 10 ns$ Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C		

Fig.10 Typical thermal response [$Z_{th(j-c)}(t)$]

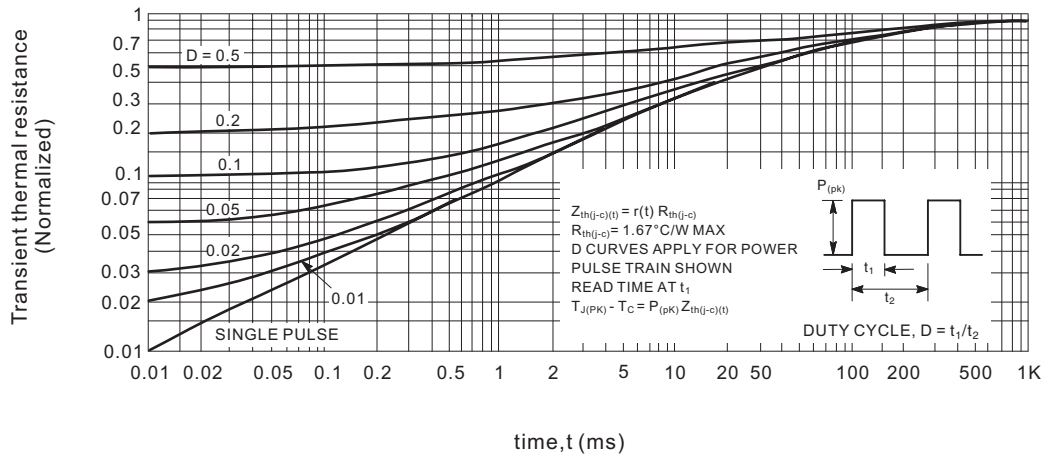
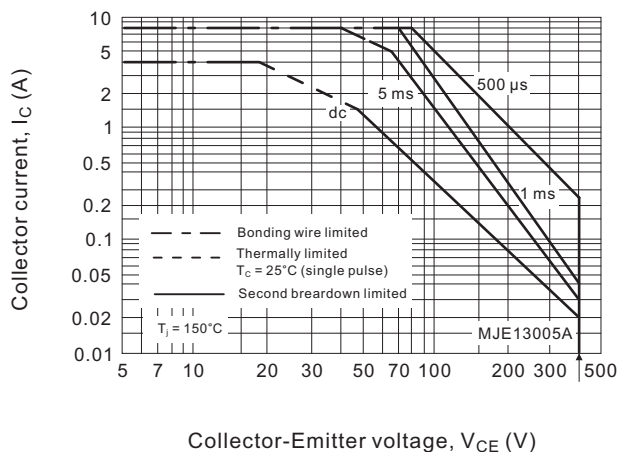


Fig.11 Forward bias safe operating area (FBSOA)



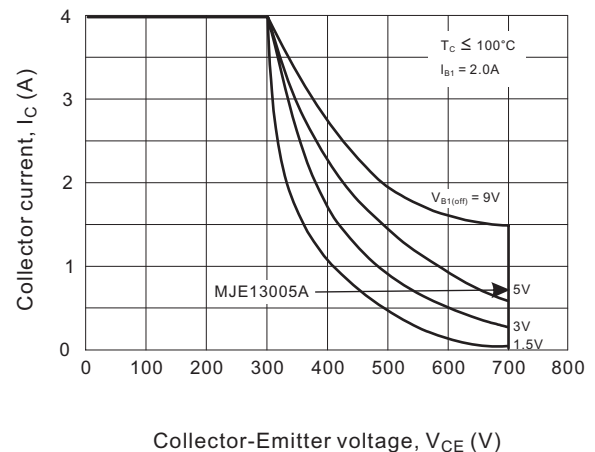
FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig.11 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Fig.11 may be found at any case temperature by using the appropriate curve on Fig.13.

$T_{J(pk)}$ may be calculated from the data in Fig.10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

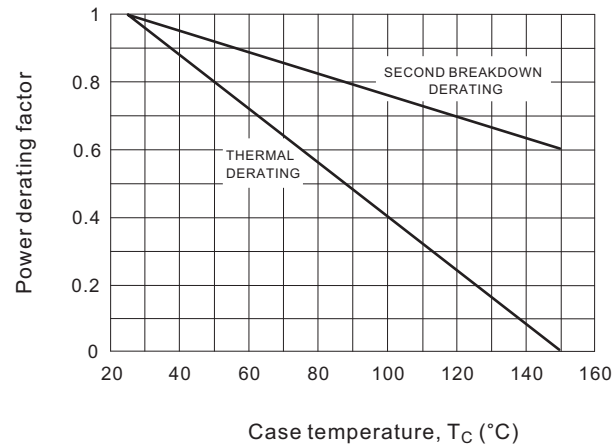
Fig.12 Reverse bias switching safe operating area (RBSOA)



REVERSE BLAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Fig.12 gives the complete RBSOA characteristics.

Fig.13 Forward bias power derating



TO-220AB

