

NSS60100DMT

60 V, 1 A, Low $V_{CE(sat)}$ PNP Transistors

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and LED lighting, power management...etc. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- NSV60100DMTWTBG – Wettable Flanks Device
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CBO}	60	Vdc
Emitter-Base Voltage	V_{EBO}	6	Vdc
Collector Current – Continuous	I_C	1	A
Collector Current – Peak	I_{CM}	2	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction-to-Ambient (Notes 1 and 2)	$R_{\theta JA}$	55	$^\circ\text{C/W}$
Total Power Dissipation per Package @ $T_A = 25^\circ\text{C}$ (Note 2)	P_D	2.27	W
Thermal Resistance Junction-to-Ambient (Note 3)	$R_{\theta JA}$	69	$^\circ\text{C/W}$
Power Dissipation per Transistor @ $T_A = 25^\circ\text{C}$ (Note 3)	P_D	1.8	W
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

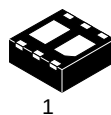
1. Per JESD51-7 with 100 mm² pad area and 2 oz. Cu (Dual Operation).
2. P_D per Transistor when both are turned on is one half of Total P_D or 1.13 Watts.
3. Per JESD51-7 with 100 mm² pad area and 2 oz. Cu (Single-Operation).



ON Semiconductor®

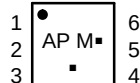
www.onsemi.com

60 Volt, 1 Amp PNP Low $V_{CE(sat)}$ Transistors



WDFN6
CASE 506AN

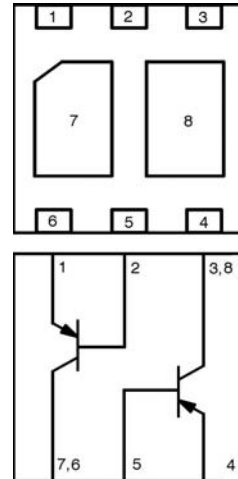
MARKING DIAGRAM



AP = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NSS60100DMTTBG	WDFN6 (Pb-Free)	3000/Tape & Reel
NSV60100DMTWTBG	WDFN6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NSS60100DMT

Table 1. ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = -10\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	-60			V
Collector-Base Breakdown Voltage ($I_C = -0.1\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	-80			V
Emitter-Base Breakdown Voltage ($I_E = -0.1\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	-6			V
Collector Cutoff Current ($V_{CB} = -60\text{ V}$, $I_E = 0$)	I_{CBO}			-100	nA
Emitter Cutoff Current ($V_{BE} = -5.0\text{ V}$)	I_{EBO}			-100	nA
ON CHARACTERISTICS					
DC Current Gain (Note 4) ($I_C = -100\text{ mA}$, $V_{CE} = -2.0\text{ V}$) ($I_C = -500\text{ mA}$, $V_{CE} = -2.0\text{ V}$) ($I_C = -1\text{ A}$, $V_{CE} = -2.0\text{ V}$) ($I_C = -2\text{ A}$, $V_{CE} = -2.0\text{ V}$)	h_{FE}	150 120 90 40	230 180 140 80		
Collector-Emitter Saturation Voltage (Note 4) ($I_C = -500\text{ mA}$, $I_B = -50\text{ mA}$) ($I_C = -1\text{ A}$, $I_B = -50\text{ mA}$) ($I_C = -1\text{ A}$, $I_B = -100\text{ mA}$)	$V_{CE(sat)}$		-0.115 -0.250 -0.200	-0.160 -0.350 -0.300	V
Base-Emitter Saturation Voltage (Note 4) ($I_C = -500\text{ mA}$, $I_B = -50\text{ mA}$) ($I_C = -1\text{ A}$, $I_B = -50\text{ mA}$) ($I_C = -1\text{ A}$, $I_B = -100\text{ mA}$)	$V_{BE(sat)}$			-1.0 -1.0 -1.1	V
Base-Emitter Turn-on Voltage (Note 4) ($I_C = 500\text{ mA}$, $I_B = 50\text{ mA}$)	$V_{BE(on)}$			-0.9	V
DYNAMIC CHARACTERISTICS					
Output Capacitance ($V_{CB} = 10\text{ V}$, $f = 1.0\text{ MHz}$)	C_{obo}		18		pF
Cutoff Frequency ($I_C = 50\text{ mA}$, $V_{CE} = 2.0\text{ V}$, $f = 100\text{ MHz}$)	f_T		155		MHz
SWITCHING TIMES					
Delay Time ($V_{CC} = -10\text{ V}$, $I_C = -0.5\text{ A}$, $I_{B1} = -25\text{ mA}$, $I_{B2} = 25\text{ mA}$)	t_d		15		ns
Rise Time ($V_{CC} = -10\text{ V}$, $I_C = -0.5\text{ A}$, $I_{B1} = -25\text{ mA}$, $I_{B2} = 25\text{ mA}$)	t_r		13		ns
Storage Time ($V_{CC} = -10\text{ V}$, $I_C = -0.5\text{ A}$, $I_{B1} = -25\text{ mA}$, $I_{B2} = 25\text{ mA}$)	t_s		360		ns
Fall Time ($V_{CC} = -10\text{ V}$, $I_C = -0.5\text{ A}$, $I_{B1} = -25\text{ mA}$, $I_{B2} = 25\text{ mA}$)	t_f		22		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Condition: Pulse Width = 300 μsec , Duty Cycle $\leq 2\%$

TYPICAL CHARACTERISTICS

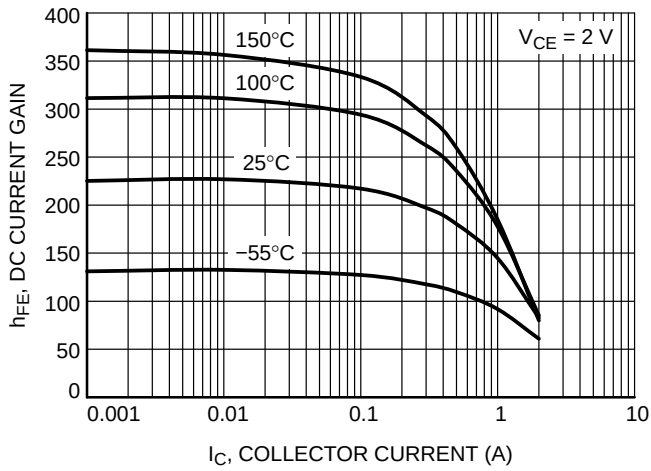


Figure 1. DC Current Gain

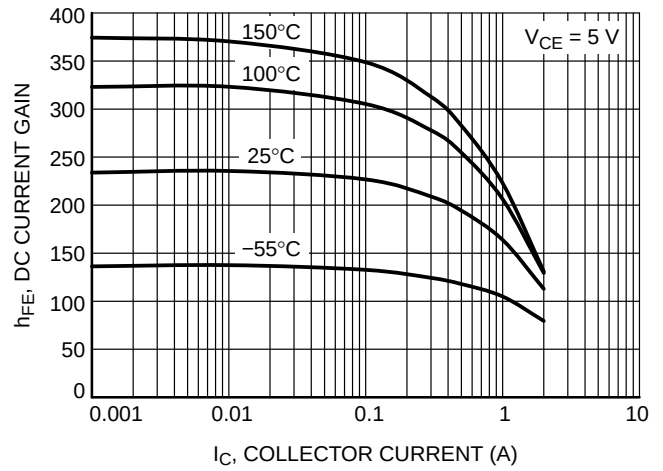


Figure 2. DC Current Gain

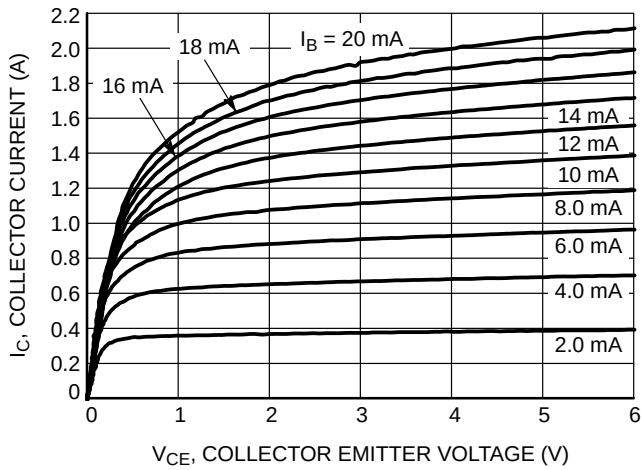


Figure 3. Collector Current as a Function of Collector Emitter Voltage

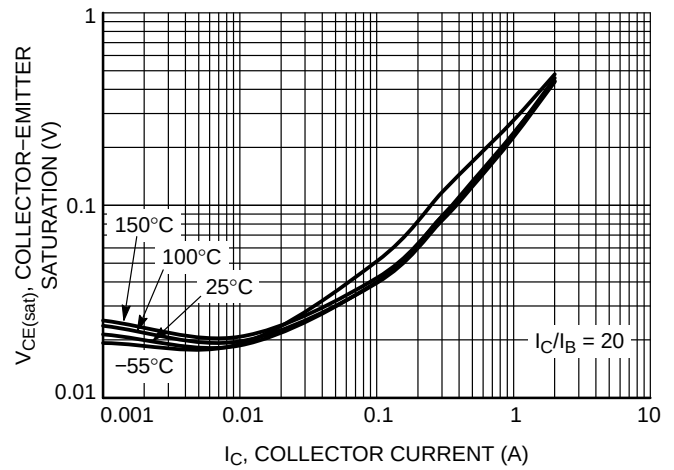


Figure 4. Collector-Emitter Saturation Voltage

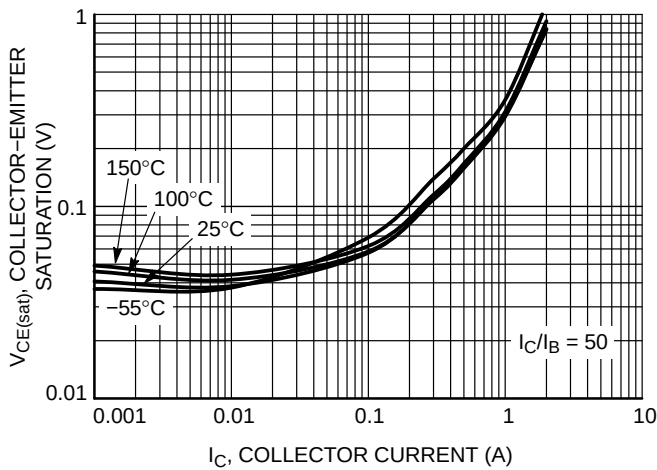


Figure 5. Collector-Emitter Saturation Voltage

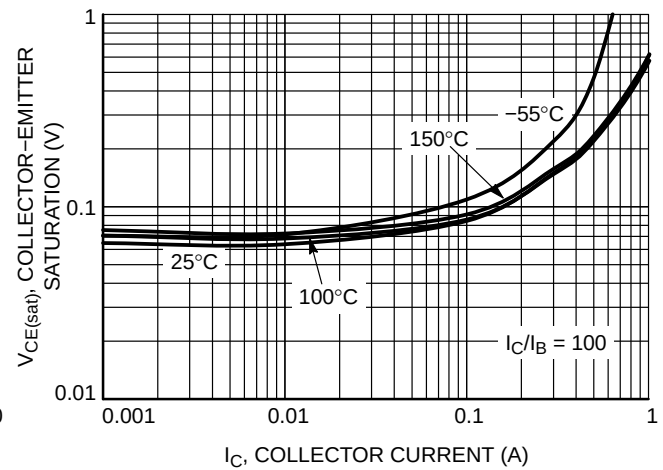


Figure 6. Collector-Emitter Saturation Voltage

TYPICAL CHARACTERISTICS

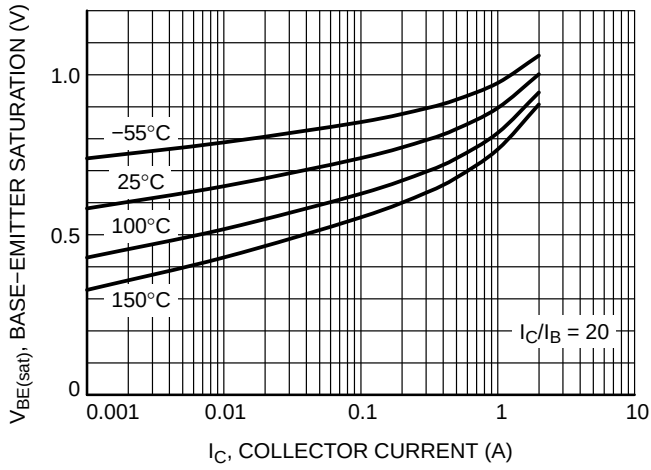


Figure 7. Base-Emitter Saturation Voltage

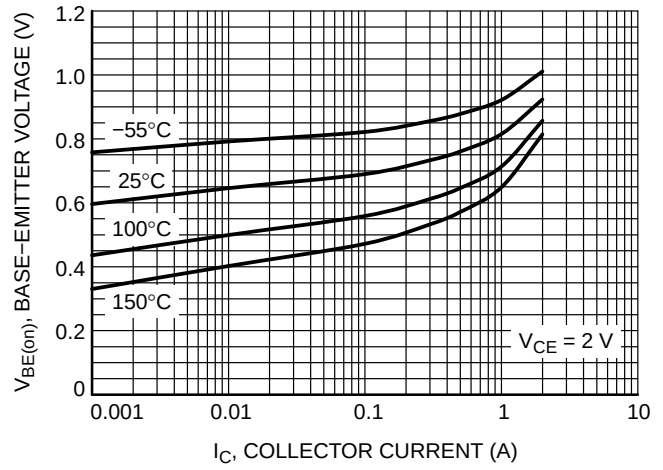


Figure 8. Base-Emitter "ON" Voltage

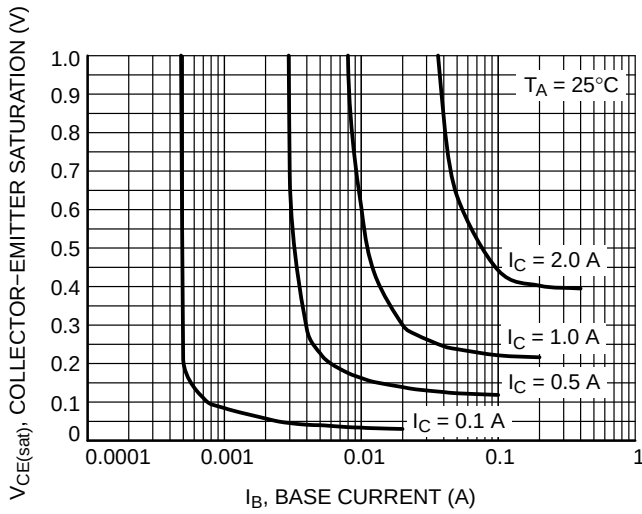


Figure 9. Collector Saturation Region

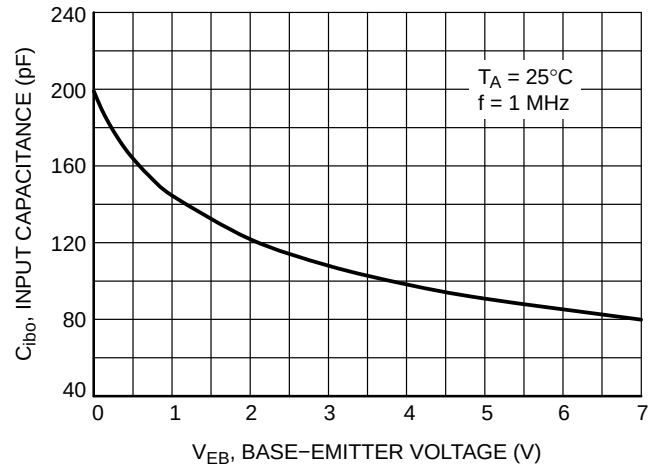


Figure 10. Input Capacitance

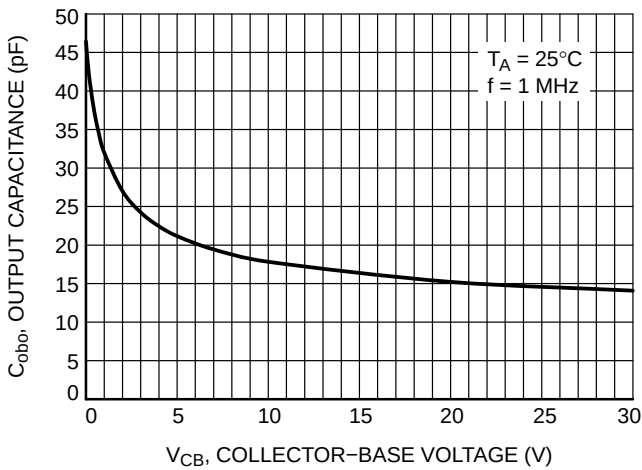


Figure 11. Output Capacitance

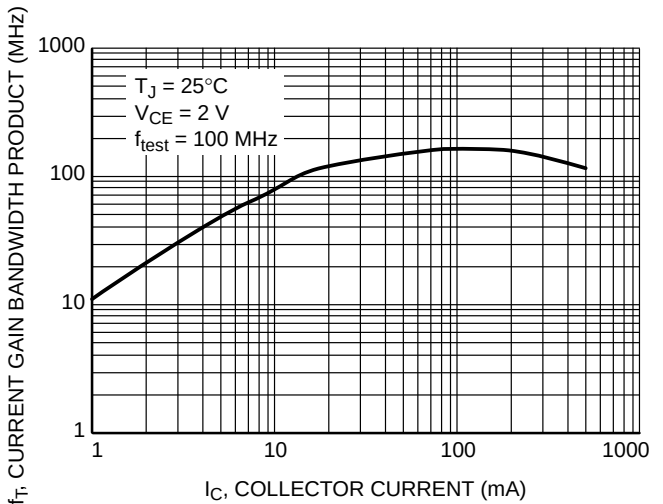


Figure 12. f_T , Current Gain Bandwidth Product

NSS60100DMT

TYPICAL CHARACTERISTICS

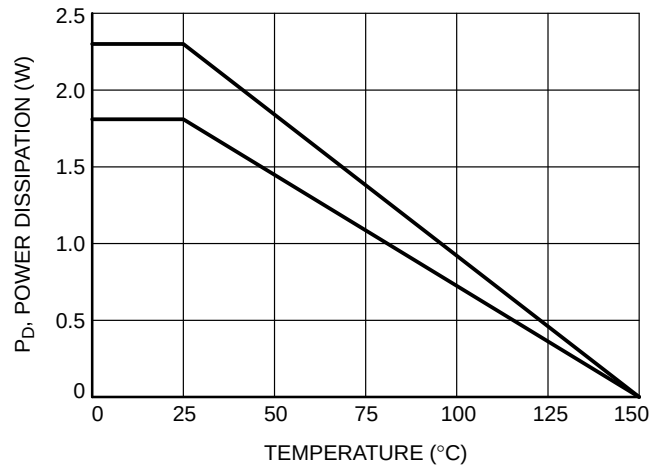


Figure 13. Power Derating

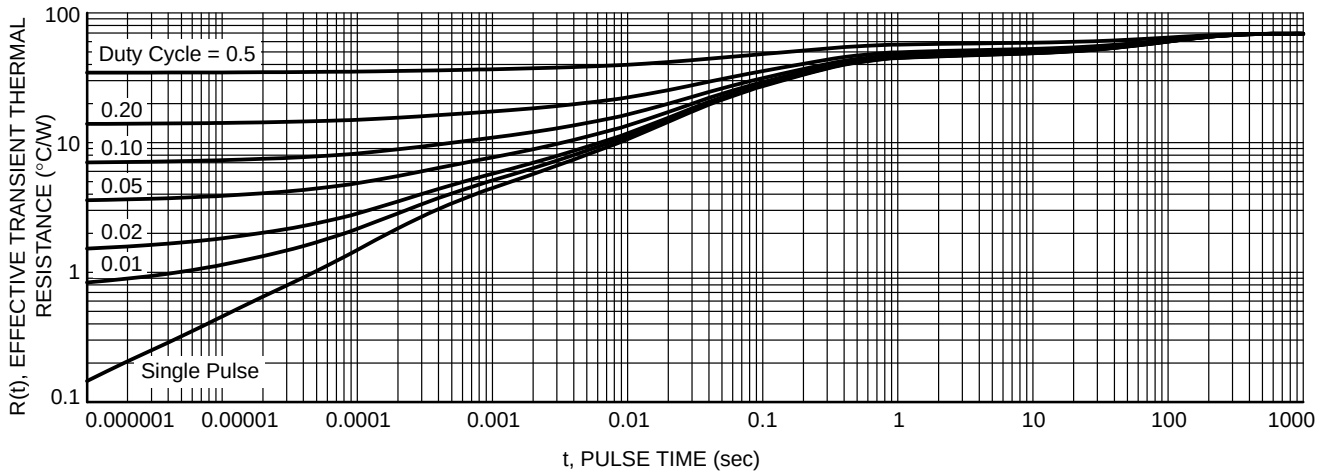


Figure 14. Thermal Resistance by Transistor

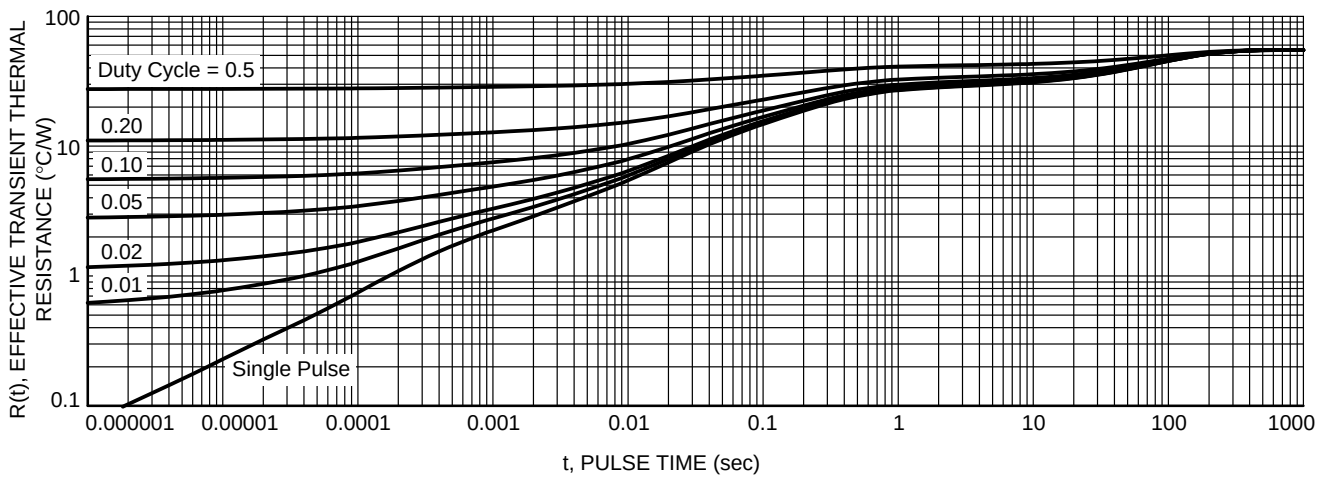
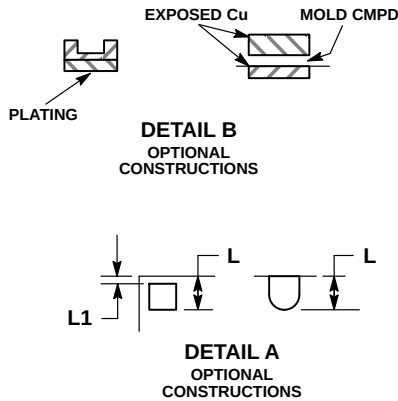
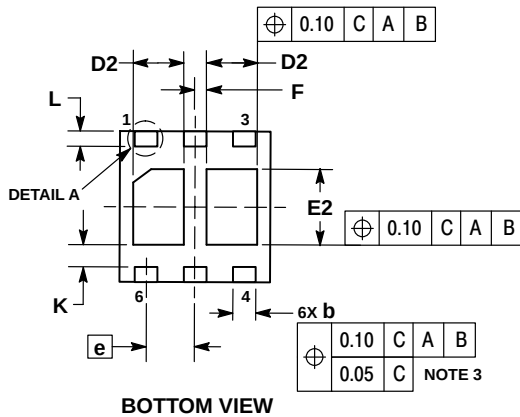
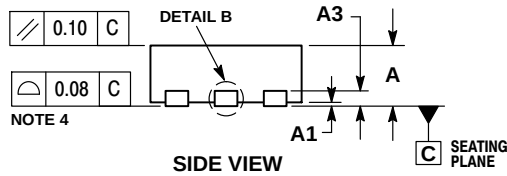
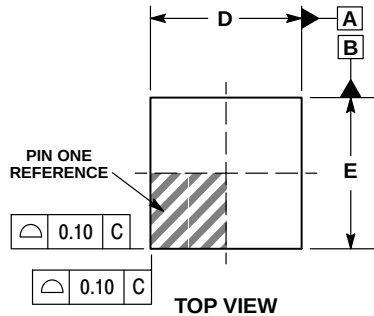


Figure 15. Thermal Resistance for Both Transistors

NSS60100DMT

PACKAGE DIMENSIONS

WDFN6 2x2, 0.65P
CASE 506AN
ISSUE F

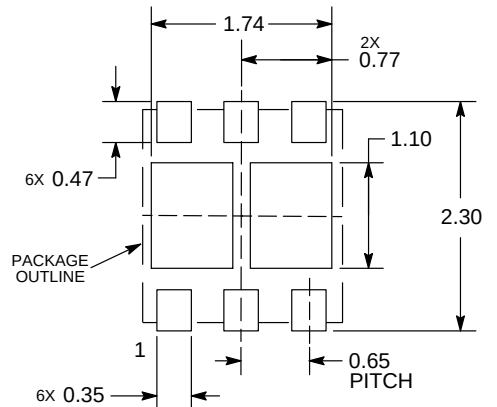


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.15 BSC	
K	0.25 REF	
L	0.20	0.30
L1	---	0.10

SOLDERMASK DEFINED MOUNTING FOOTPRINT



ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NSS60100DMT/D