

2SJ549(L), 2SJ549(S)

Silicon P Channel MOS FET

REJ03G0896-0400

Rev.4.00

Jun 05, 2006

Description

High speed power switching

Features

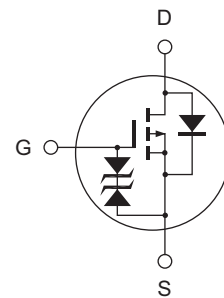
- Low on-resistance
 $R_{DS(on)} = 0.11 \Omega$ typ.
- Low drive current
- 4 V gate drive devices
- High speed switching

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))



RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK (S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Value | Unit |
|---|--|-------------|------|
| Drain to source voltage | V _{DSS} | -60 | V |
| Gate to source voltage | V _{GSS} | ±20 | V |
| Drain current | I _D | -12 | A |
| Drain peak current | I _{D (pulse)} ^{Note 1} | -48 | A |
| Body to drain diode reverse drain current | I _{DR} | -12 | A |
| Avalanche current | I _{AP} ^{Note 3} | -12 | A |
| Avalanche energy | E _{AR} ^{Note 3} | 12 | mJ |
| Channel dissipation | P _{ch} ^{Note 2} | 50 | W |
| Channel temperature | T _{ch} | 150 | °C |
| Storage temperature | T _{stg} | -55 to +150 | °C |

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at T_c = 25°C3. Value at T_{ch} = 25°C, R_g ≥ 50 Ω

Electrical Characteristics

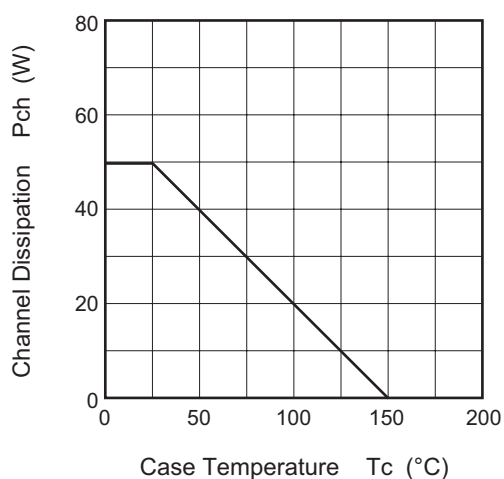
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|-----------------------|------|------|------|------|--|
| Drain to source breakdown voltage | V _{(BR) DSS} | -60 | — | — | V | I _D = -10 mA, V _{GS} = 0 |
| Gate to source breakdown voltage | V _{(BR) GSS} | ±20 | — | — | V | I _G = ±100 μA, V _{DS} = 0 |
| Zero gate voltage drain current | I _{DSS} | — | — | -10 | μA | V _{DS} = -60 V, V _{GS} = 0 |
| Gate to source leak current | I _{GSS} | — | — | ±10 | μA | V _{GS} = ±16 V, V _{DS} = 0 |
| Gate to source cutoff voltage | V _{GS (off)} | -1.0 | — | -2.0 | V | I _D = -1 mA, V _{DS} = -10 V |
| Static drain to source on state resistance | R _{DS (on)} | — | 0.11 | 0.15 | Ω | I _D = -6 A, V _{GS} = -10 V ^{Note 4} |
| | R _{DS (on)} | — | 0.16 | 0.23 | Ω | I _D = -6 A, V _{GS} = -4 V ^{Note 4} |
| Forward transfer admittance | y _{fs} | 5 | 8 | — | S | I _D = -6 A, V _{DS} = -10 V ^{Note 4} |
| Input capacitance | C _{iss} | — | 580 | — | pF | V _{DS} = -10 V |
| Output capacitance | C _{oss} | — | 300 | — | pF | V _{GS} = 0 |
| Reverse transfer capacitance | C _{rss} | — | 85 | — | pF | f = 1 MHz |
| Turn-on delay time | t _{d (on)} | — | 10 | — | ns | V _{GS} = -10 V |
| Rise time | t _r | — | 55 | — | ns | I _D = -6 A |
| Turn-off delay time | t _{d (off)} | — | 85 | — | ns | R _L = 6 Ω |
| Fall time | t _f | — | 60 | — | ns | |
| Body to drain diode forward voltage | V _{DF} | — | -1.2 | — | V | I _F = -12 A, V _{GS} = 0 |
| Body to drain diode reverse recovery time | t _{rr} | — | 60 | — | ns | I _F = -12 A, V _{GS} = 0 di _F /dt = 50 A/μs |

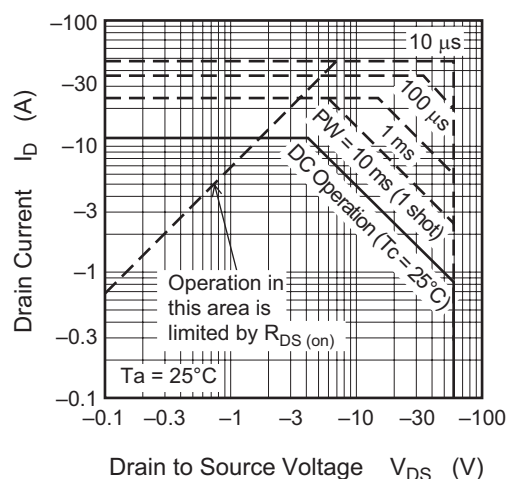
Note: 4. Pulse test

Main Characteristics

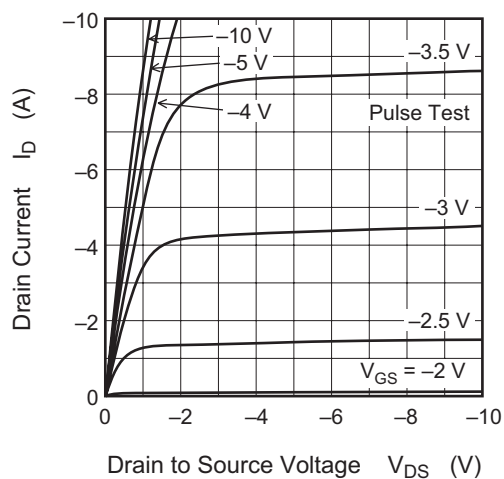
Power vs. Temperature Derating



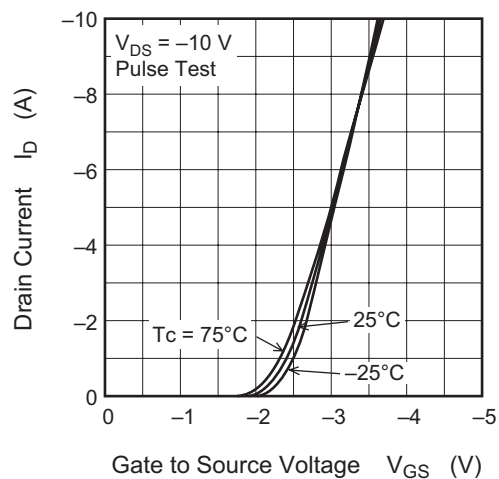
Maximum Safe Operation Area



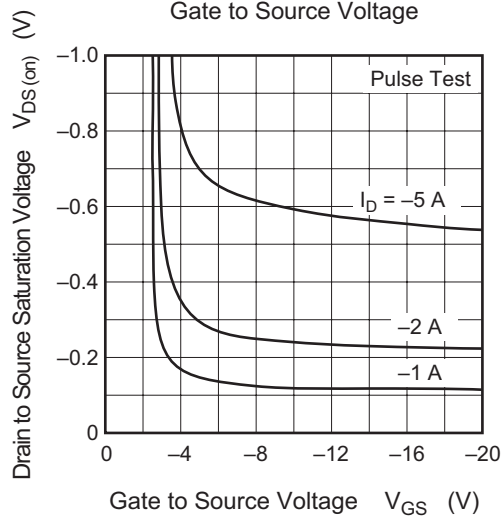
Typical Output Characteristics



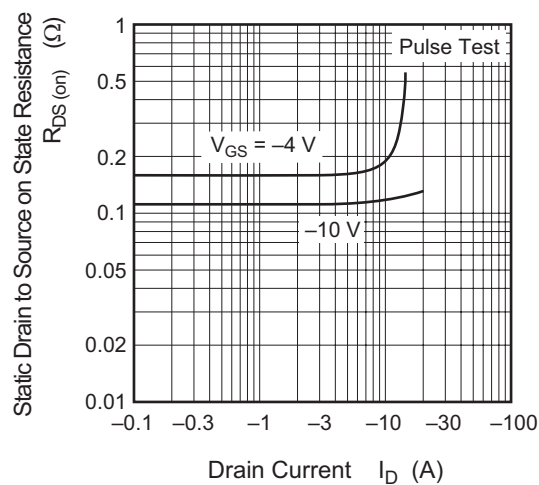
Typical Transfer Characteristics

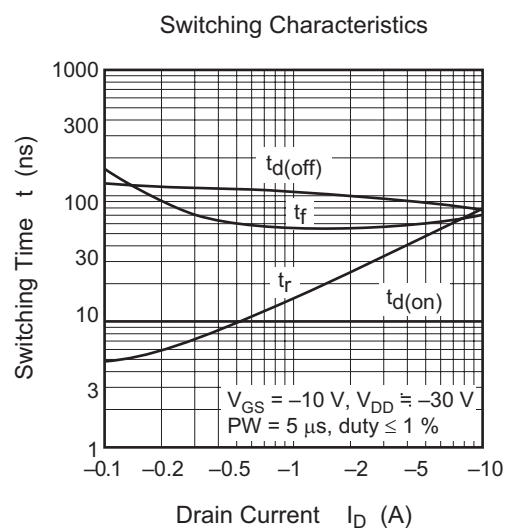
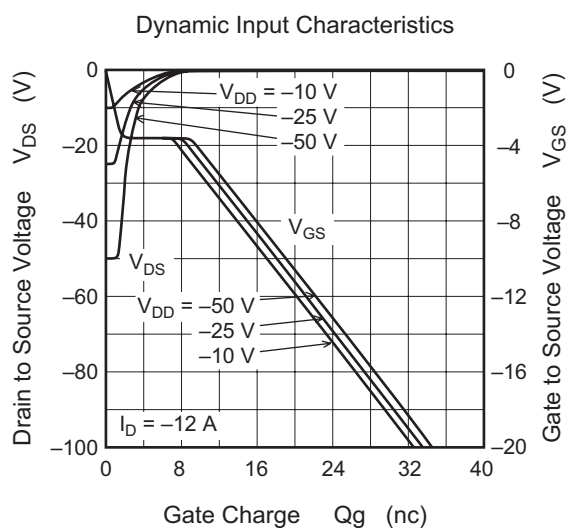
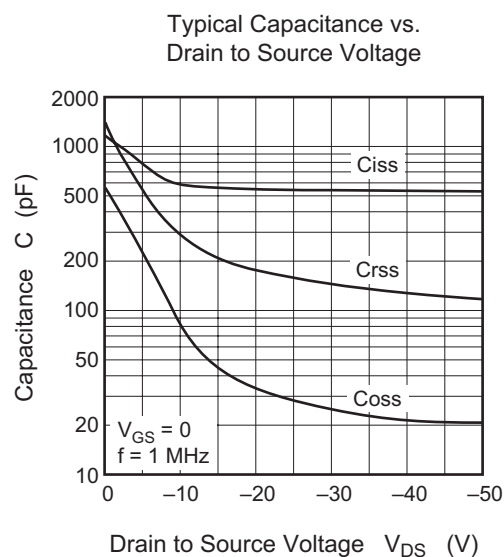
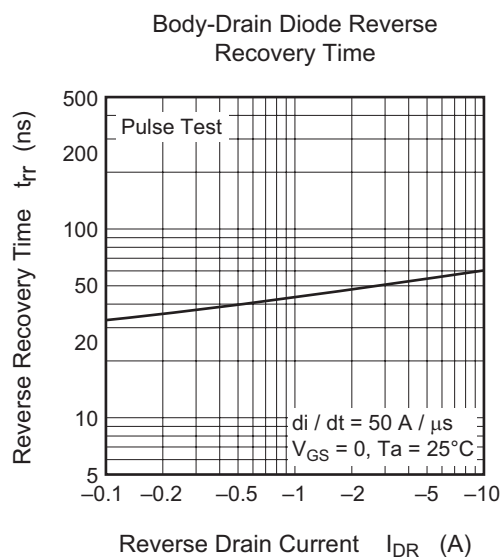
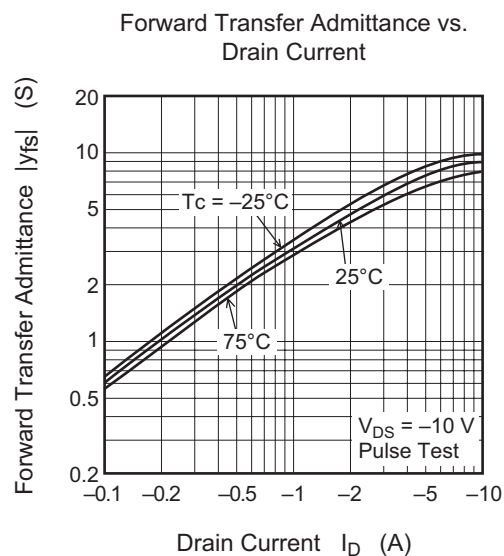
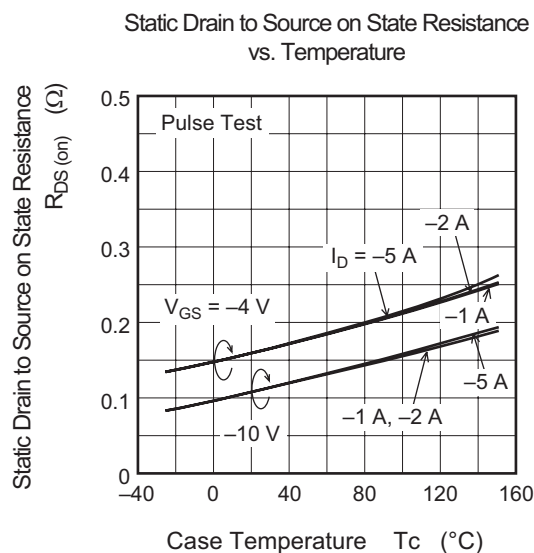


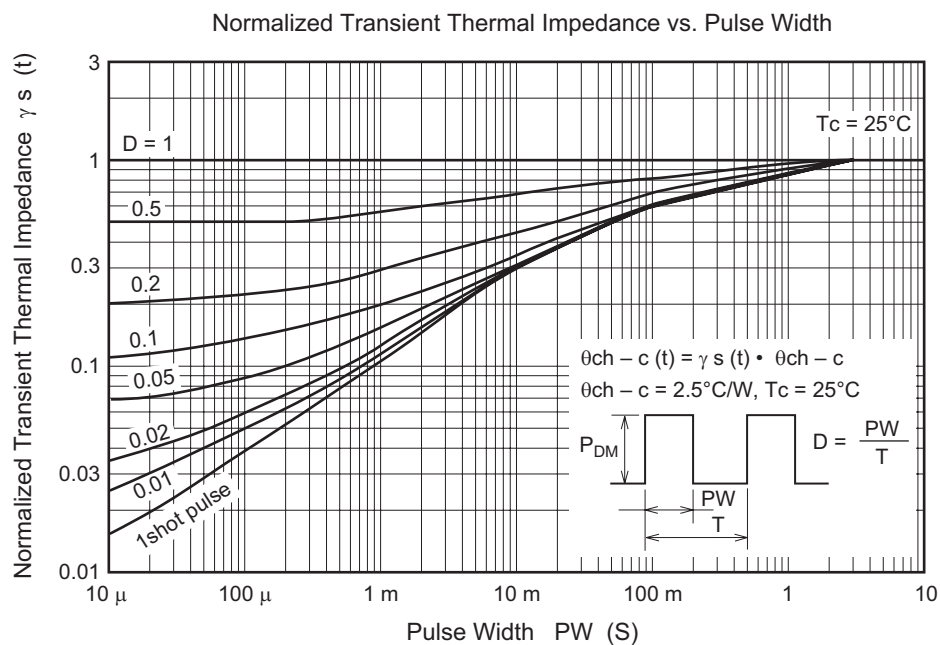
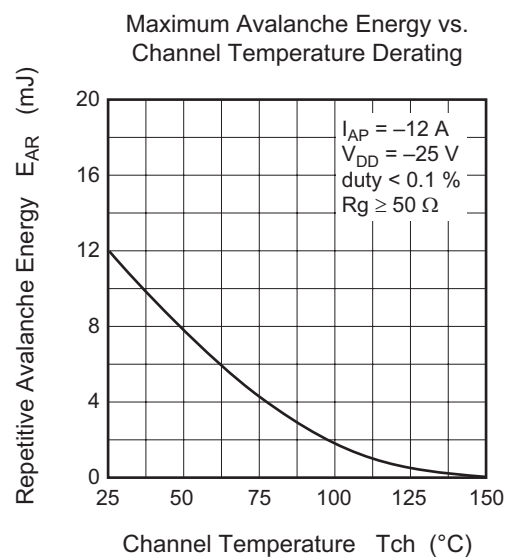
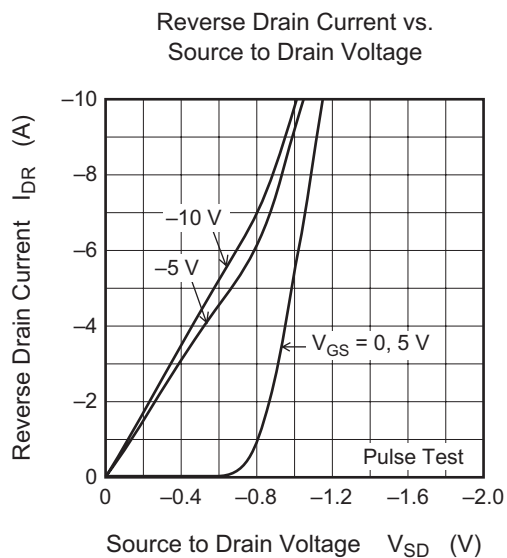
Drain to Source Saturation Voltage vs. Gate to Source Voltage



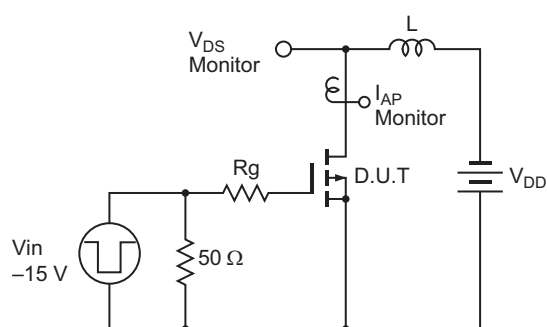
Static Drain to Source on State Resistance vs. Drain Current



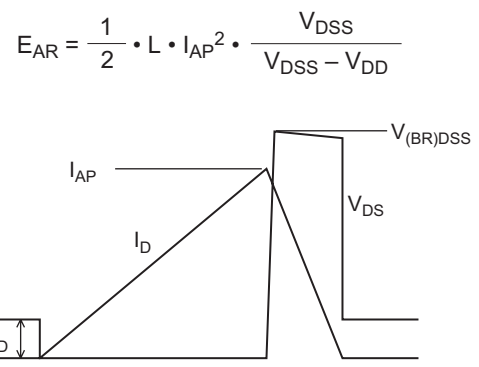


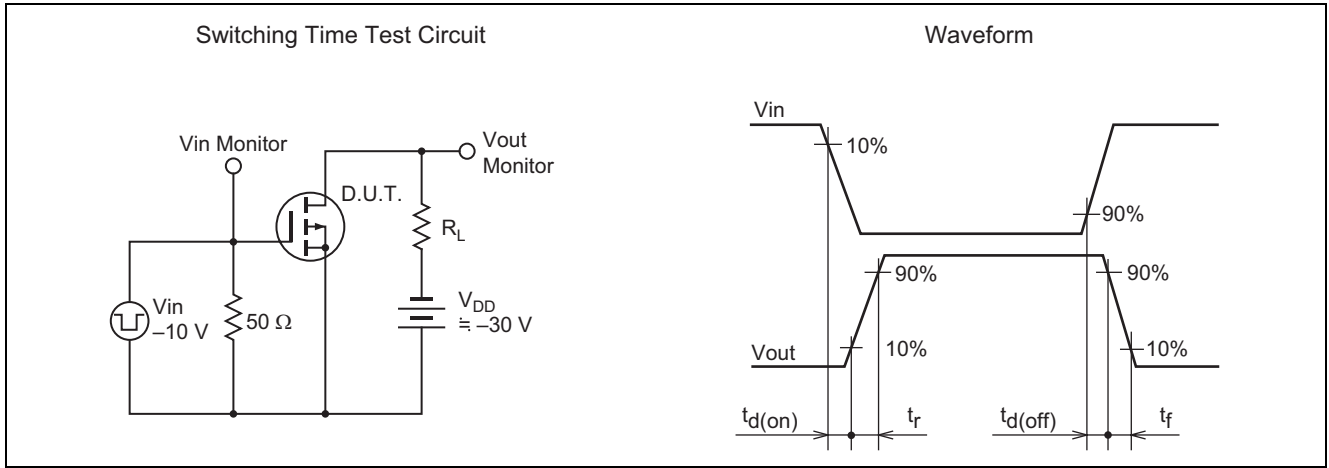


Avalanche Test Circuit

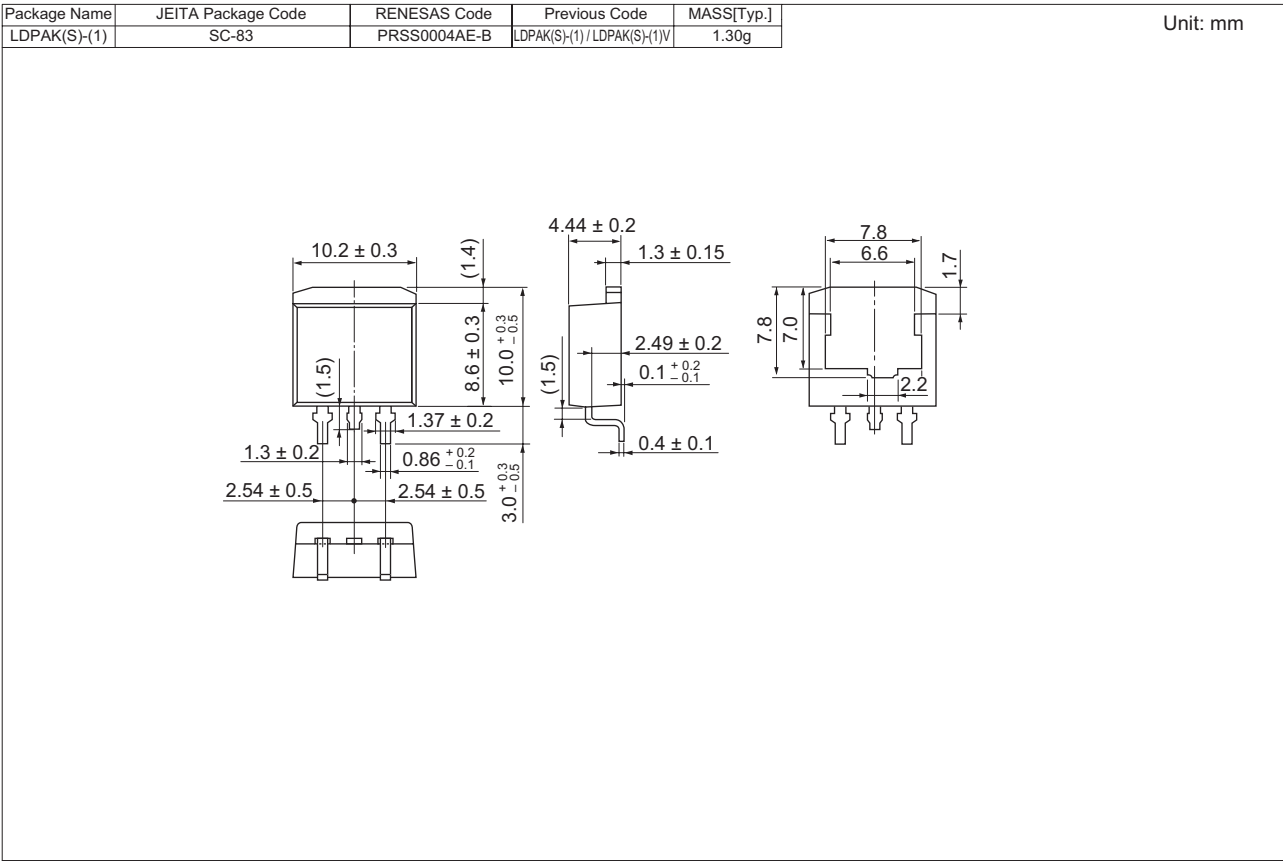
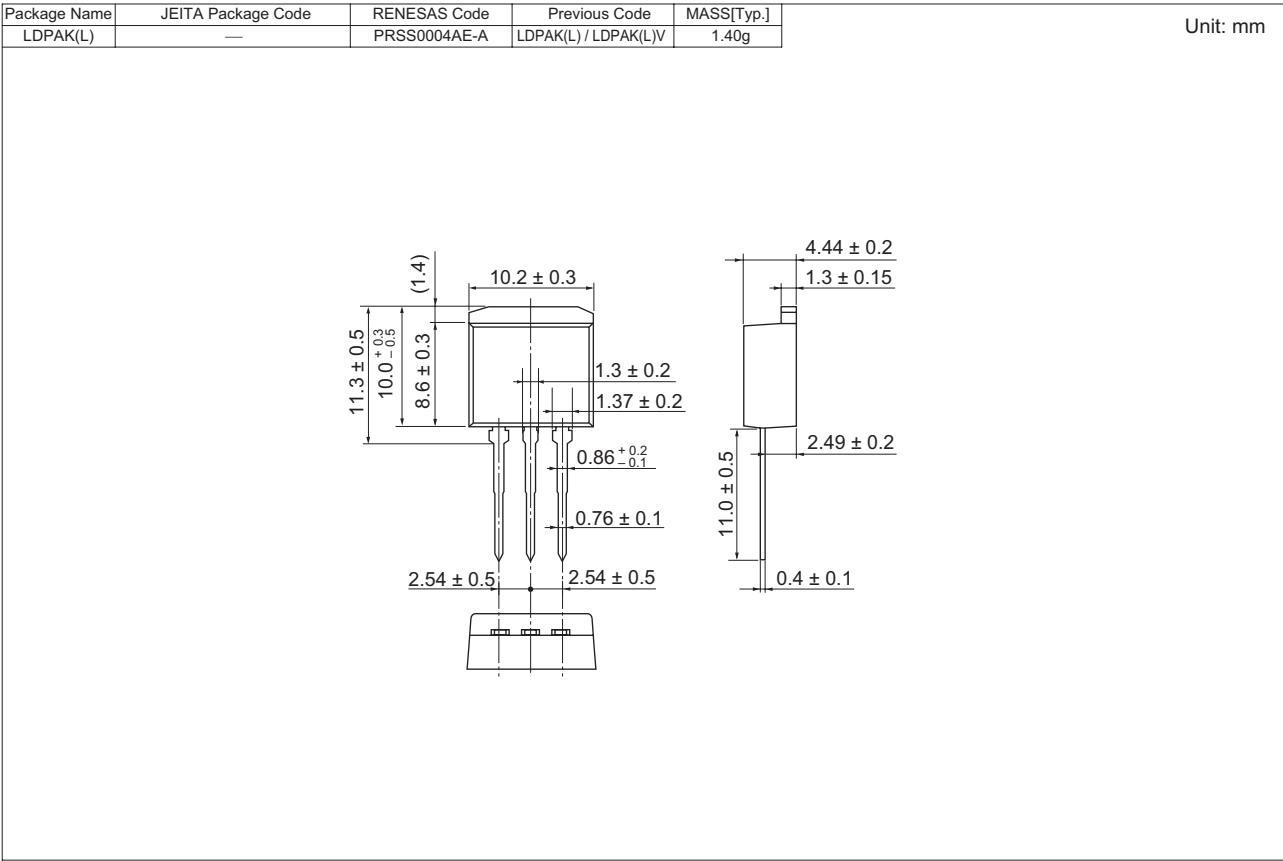


Avalanche Waveform





Package Dimensions



Ordering Information

| Part Name | Quantity | Shipping Container |
|-------------|----------|--------------------|
| 2SJ549L-E | 500 pcs | Box (Sack) |
| 2SJ549STL-E | 1000 pcs | Taping |

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