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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H5N2001LD, H5N2001LS, H5N2001LM

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1339-0600

Rev.6.00

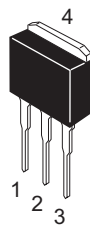
Jul 14, 2006

Features

- Low on-resistance
- Low leakage current
- High speed switching

Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))



H5N2001LD

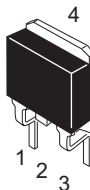
RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK (S)-(1))



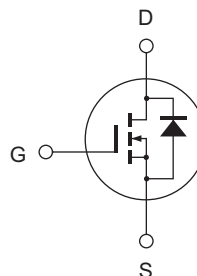
H5N2001LS

1. Gate
2. Drain
3. Source
4. Drain

RENESAS Package code: PRSS0004AE-C
(Package name: LDKPAK (S)-(2))



H5N2001LM



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	200	V
Gate to source voltage	V_{GS}	± 30	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	80	A
Body to drain diode reverse drain current	I_{DR}	20	A
Body to drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note 1}	80	A
Avalanche current	I_{AP} ^{Note 3}	20	A
Channel dissipation	P_{ch} ^{Note 2}	75	W
Channel to case Thermal Impedance	θ_{ch-c}	1.67	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. Value at $T_c = 25^\circ C$ 3. $T_{ch} \leq 150^\circ C$

Electrical Characteristics

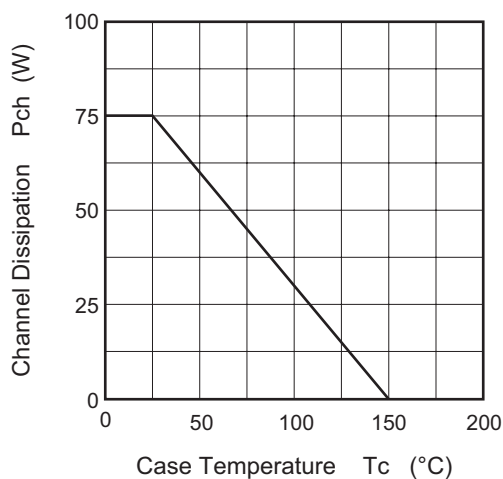
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.100	0.125	Ω	$I_D = 10 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	8	14	—	S	$I_D = 10 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	1350	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	180	—	pF	
Reverse transfer capacitance	C_{rss}	—	55	—	pF	
Turn-on delay time	$t_{d(on)}$	—	35	—	ns	$I_D = 10 \text{ A}$ $R_L = 10 \Omega$ $V_{GS} = 10 \text{ V}$ $R_g = 10 \Omega$
Rise time	t_r	—	70	—	ns	
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	t_f	—	20	—	ns	
Total gate charge	Q_g	—	44	—	nC	$V_{DD} = 160 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 20 \text{ A}$
Gate to source charge	Q_{gs}	—	8	—	nC	
Gate to drain charge	Q_{gd}	—	22	—	nC	
Body to drain diode forward voltage	V_{DF}	—	0.9	1.4	V	$I_F = 20 \text{ A}$, $V_{GS} = 0$ ^{Note 4}
Body to drain diode reverse recovery time	t_{rr}	—	140	—	ns	$I_F = 20 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu s$
Body to drain diode reverse recovery charge	Q_{rr}	—	0.7	—	μC	

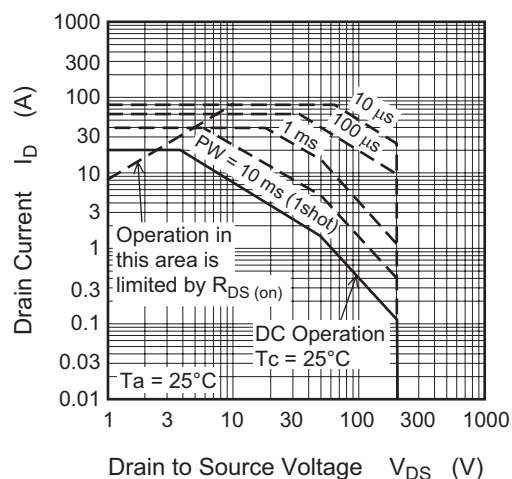
Note: 4. Pulse test

Main Characteristics

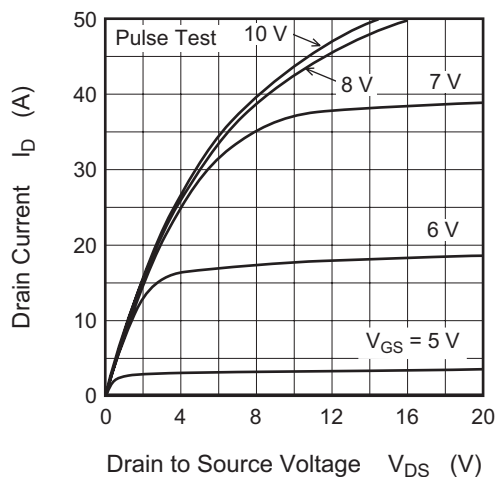
Power vs. Temperature Derating



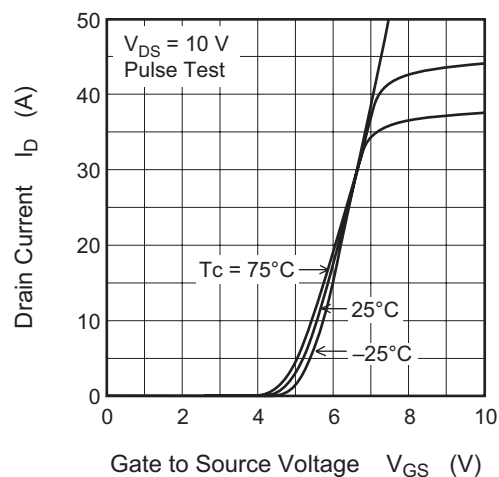
Maximum Safe Operation Area



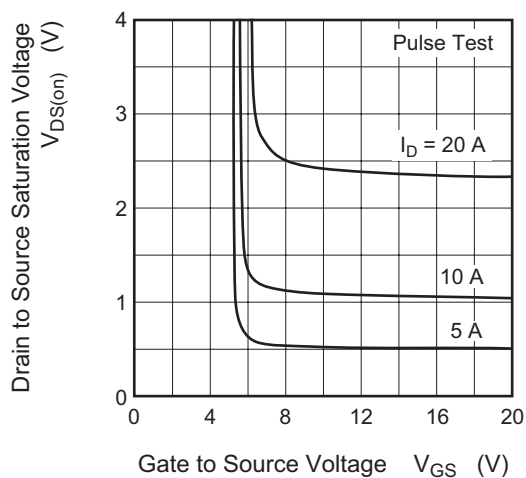
Typical Output Characteristics



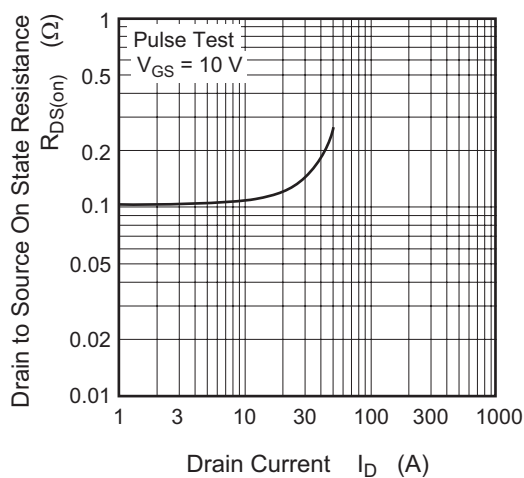
Typical Transfer Characteristics

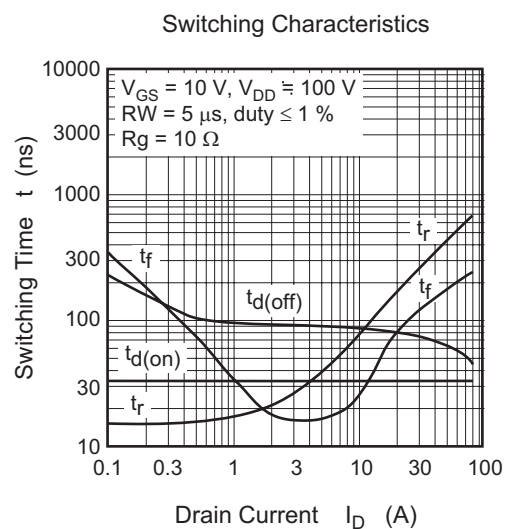
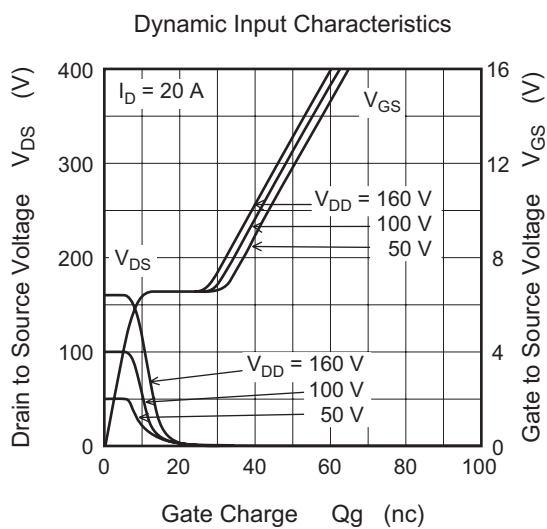
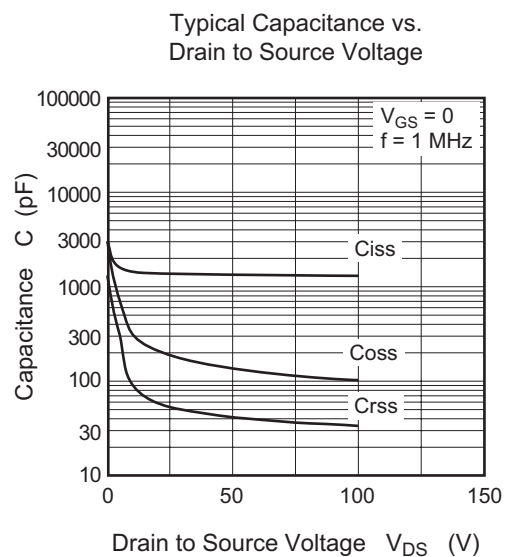
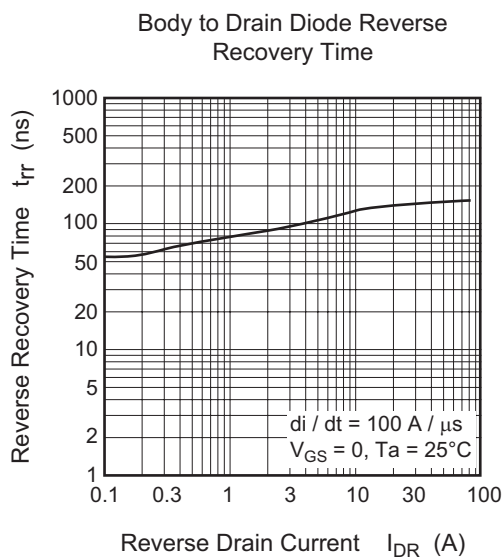
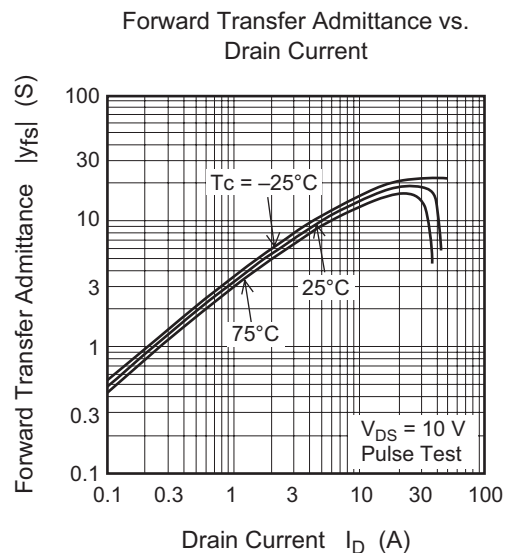
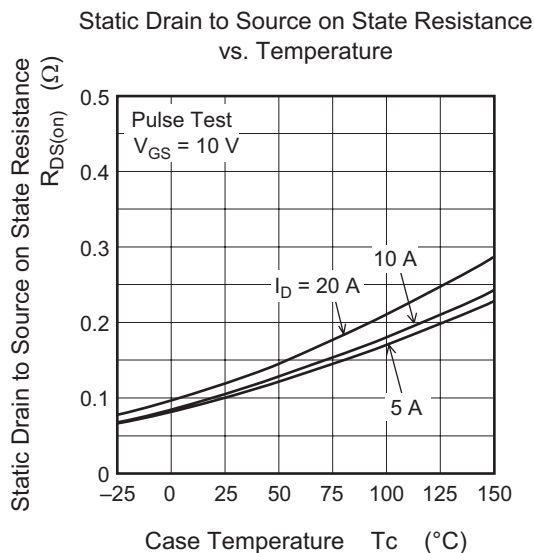


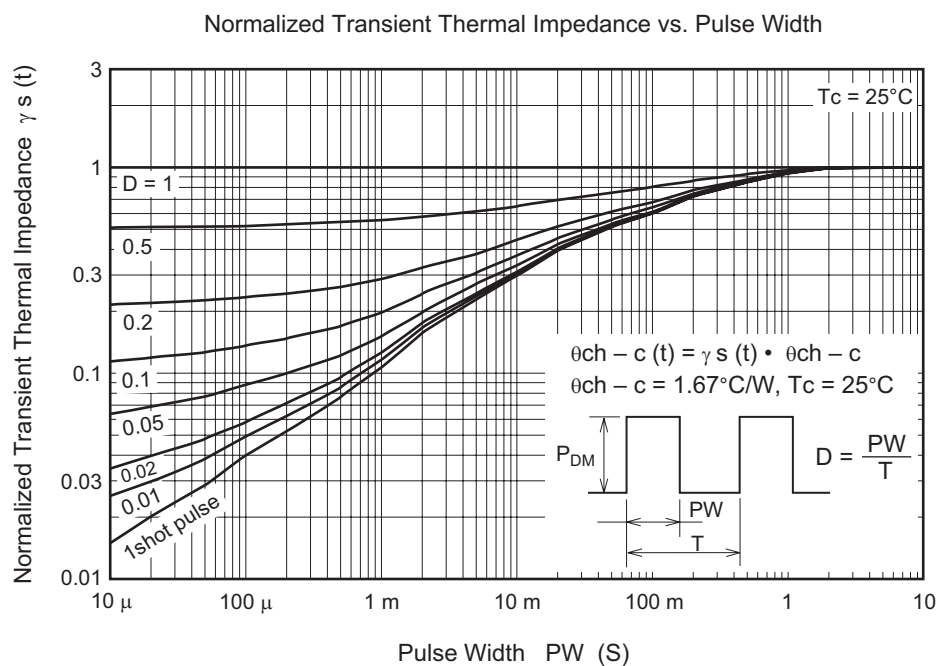
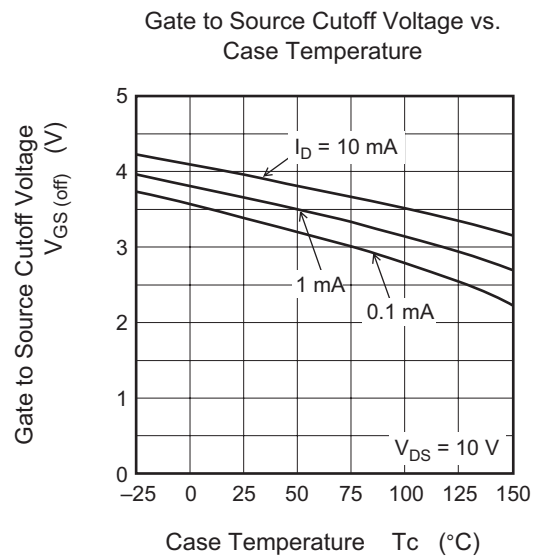
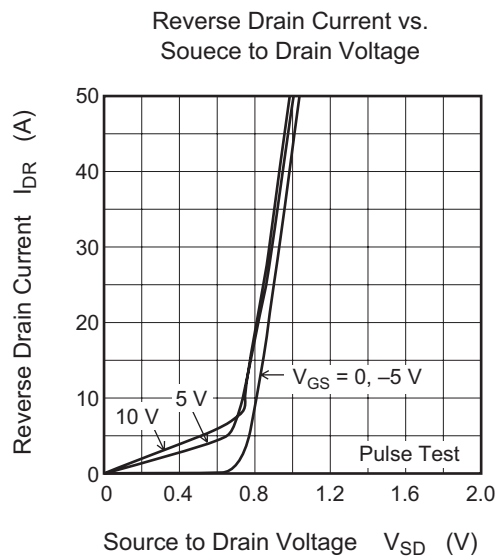
Drain to Source Saturation Voltage vs. Gate to Source Voltage



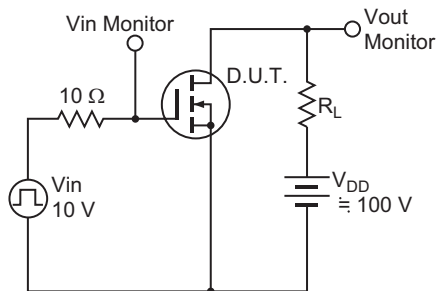
Static Drain to Source on State Resistance vs. Drain Current



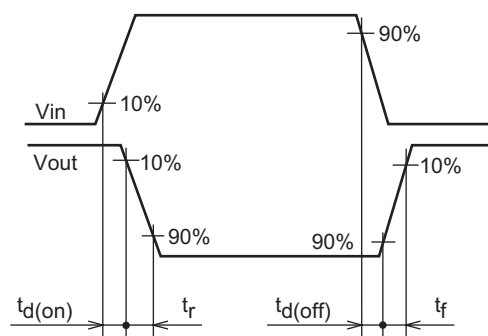




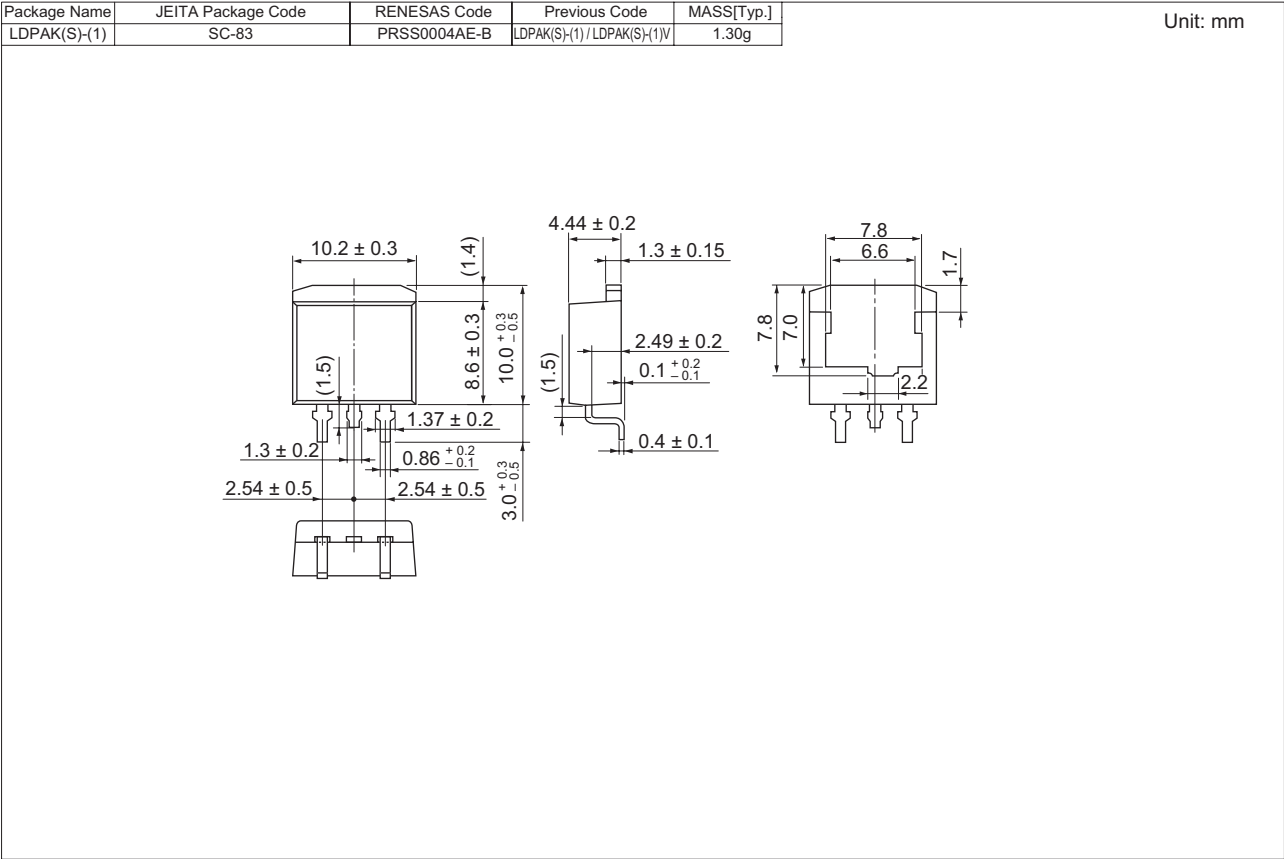
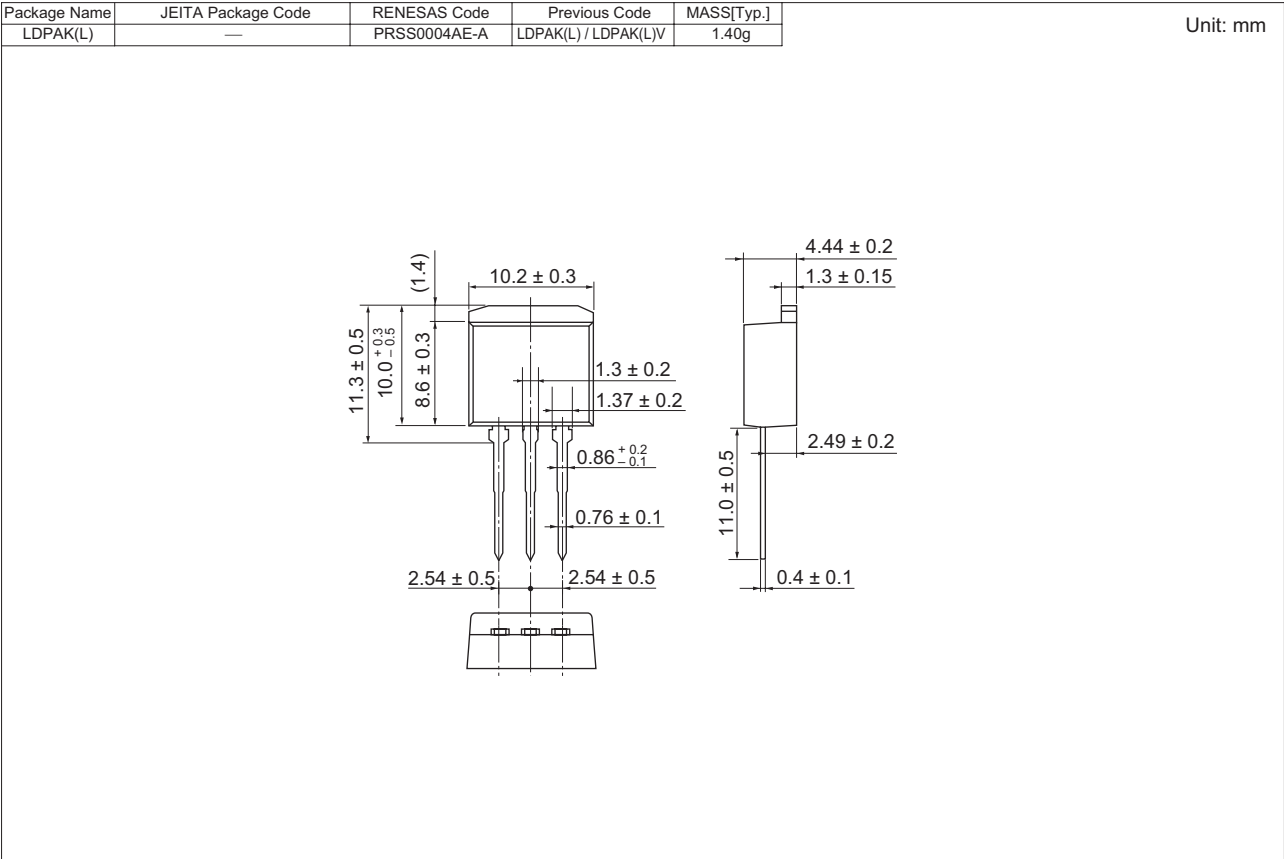
Switching Time Test Circuit



Switching Time Waveform



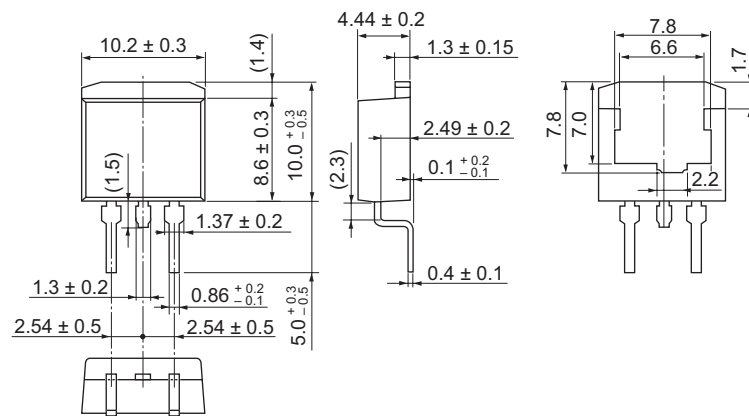
Package Dimensions



H5N2001LD, H5N2001LS, H5N2001LM

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBAK(S)-(2)	—	PRSS0004AE-C	LDBAK(S)-(2) / LDBAK(S)-(2)V	1.35g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
H5N2001LD-E	500 pcs	Box (Conductive Sack)
H5N2001LSTL-E	1000 pcs	Taping
H5N2001LMTL-E	1000 pcs	Taping

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