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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H5N5006LD, H5N5006LS, H5N5006LM

Silicon N Channel MOS FET
High Speed Power Switching

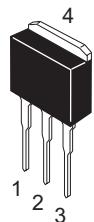
REJ03G1115-0100
(Previous: ADE-208-1549)
Rev.1.00
Apr 07, 2006

Features

- Low on-resistance
- Low leakage current
- High speed switching
- Low gate charge
- Avalanche ratings

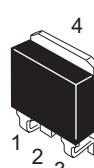
Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDPAK (L))



H5N5006LD

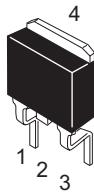
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(Package name: LDPAK (S)-(1))



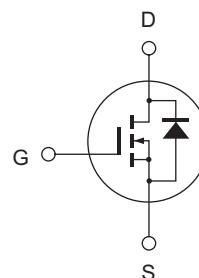
H5N5006LS

1. Gate
2. Drain
3. Source
4. Drain

RENESAS Package code: PRSS0004AE-C
(Package name: LDPAK (S)-(2))



H5N5006LM



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	500	V
Gate to source voltage	V _{GSS}	±30	V
Drain current	I _D	3.5	A
Drain peak current	I _D (pulse) ^{Note 1}	14	A
Body to drain diode reverse drain current	I _{DR}	3.5	A
Avalanche current	I _{AP} ^{Note 3}	3.5	A
Channel dissipation	P _{ch} ^{Note 2}	50	W
Channel to case Thermal Impedance	θ _{ch-c}	2.5	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
 2. Value at T_c = 25°C
 3. T_{ch} ≤ 150°C

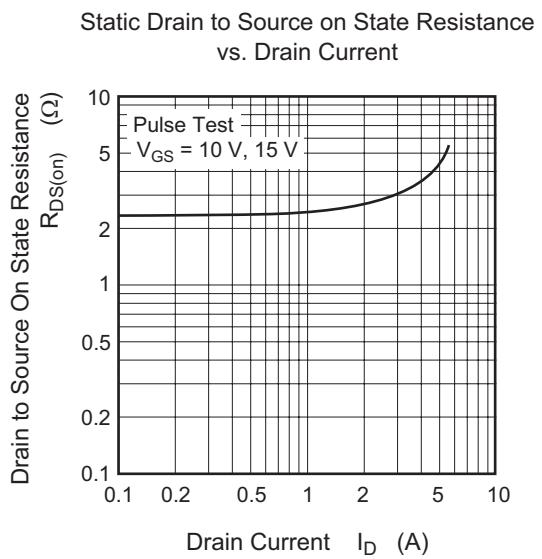
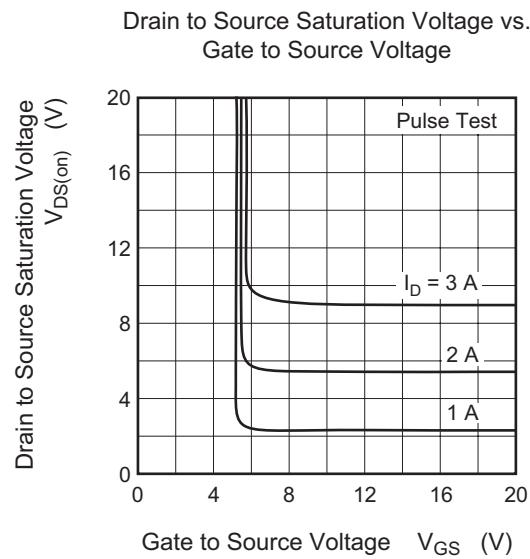
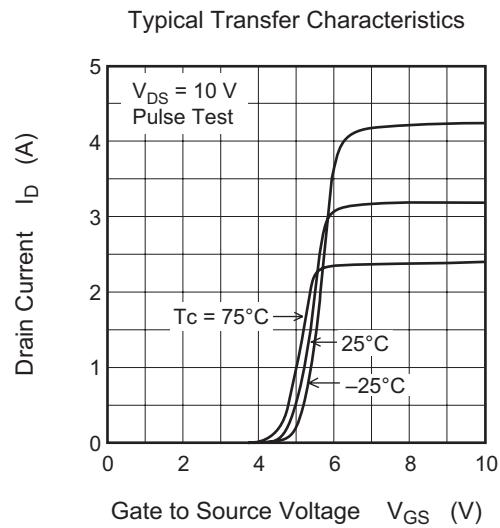
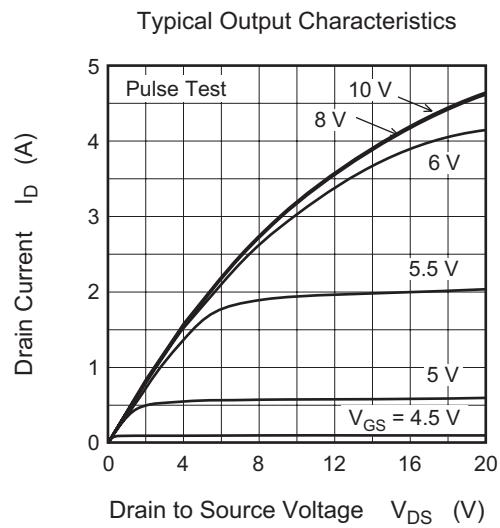
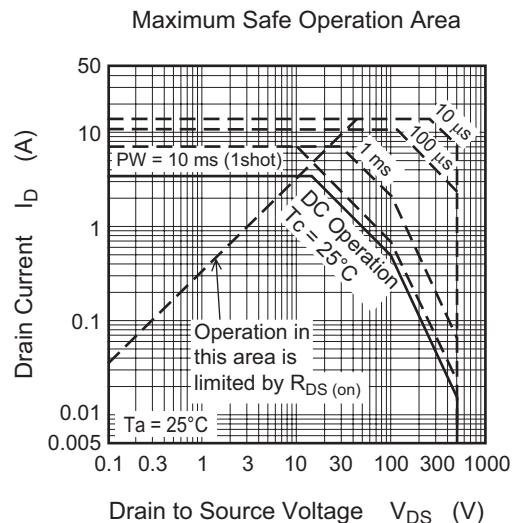
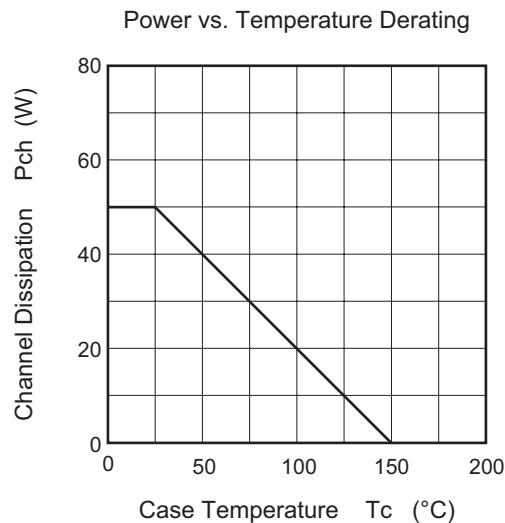
Electrical Characteristics

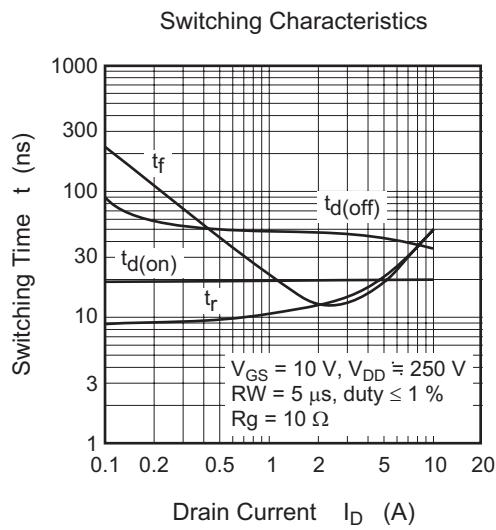
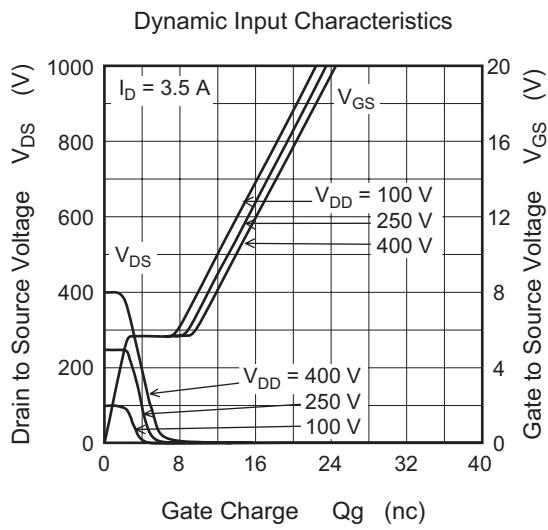
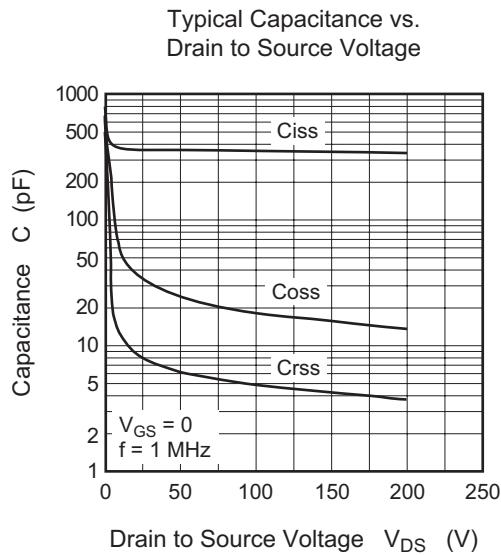
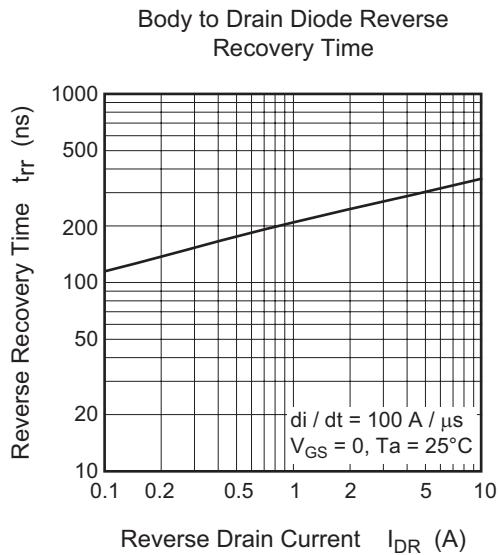
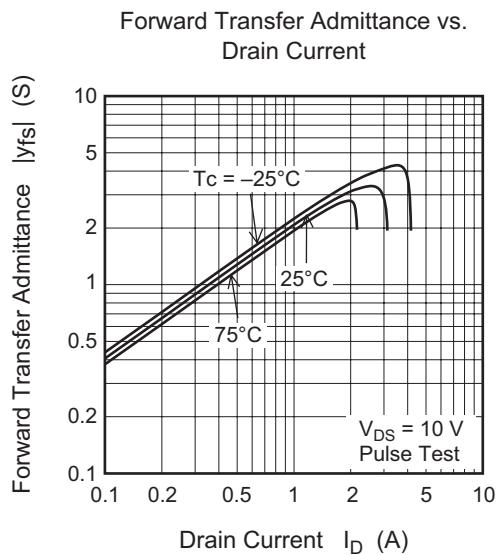
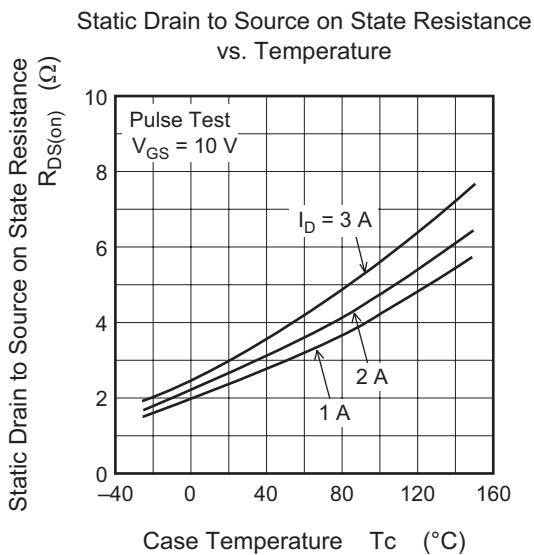
(Ta = 25°C)

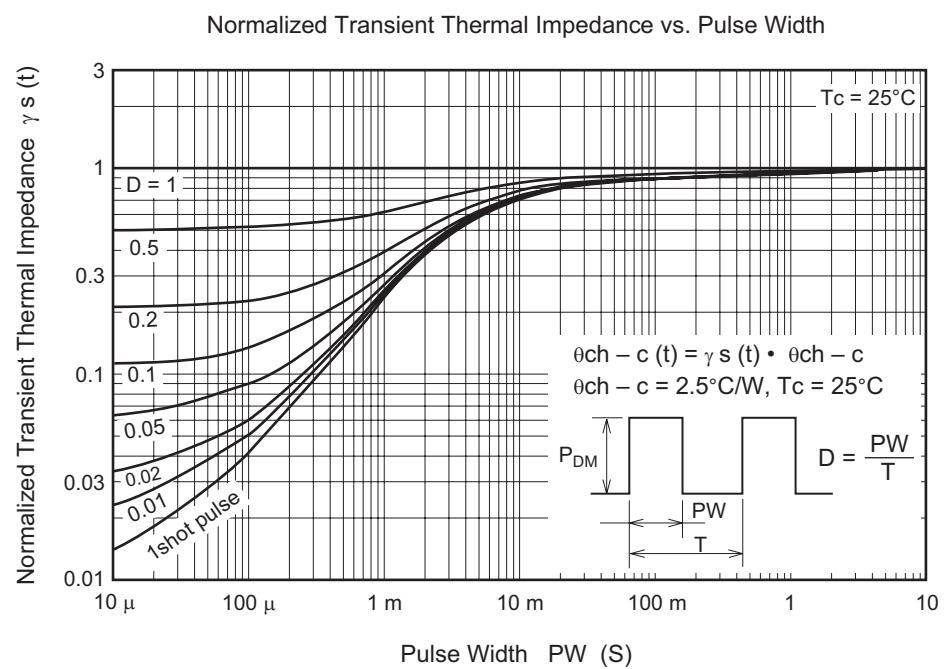
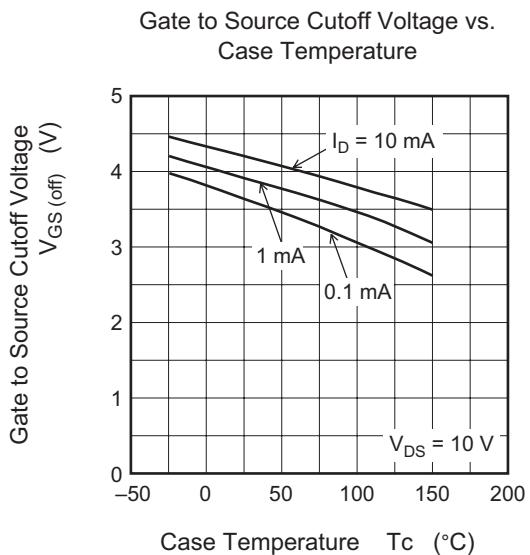
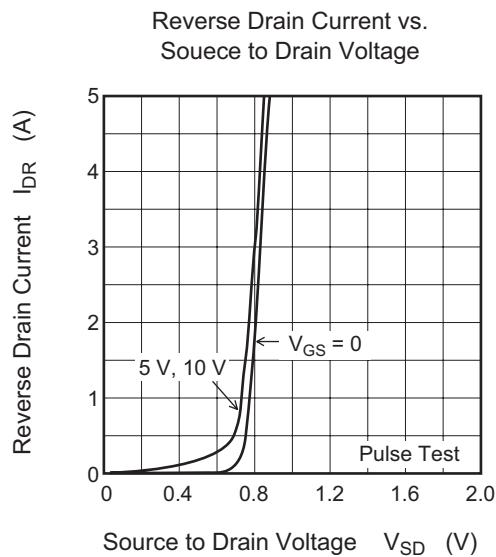
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	500	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±0.1	µA	V _{GS} = ±30 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	1	µA	V _{DS} = 500 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS} (off)	3.0	—	4.5	V	I _D = 1 mA, V _{DS} = 10 V
Static drain to source on state resistance	R _{D5} (on)	—	2.5	3.0	Ω	I _D = 1.75 A, V _{GS} = 10 V ^{Note 4}
Forward transfer admittance	Y _{fs}	1.8	3.0	—	S	I _D = 1.75 A, V _{DS} = 10 V ^{Note 4}
Input capacitance	C _{iss}	—	365	—	pF	V _{DS} = 25 V
Output capacitance	C _{oss}	—	35	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	8	—	pF	f = 1 MHz
Turn-on delay time	t _d (on)	—	20	—	ns	V _{DD} ≈ 250 V, I _D = 1.75 A
Rise time	t _r	—	13	—	ns	R _L = 143 Ω
Turn-off delay time	t _d (off)	—	48	—	ns	V _{GS} = 10 V
Fall time	t _f	—	14	—	ns	R _g = 10 Ω
Total gate charge	Q _g	—	14	—	nC	V _{DD} = 400 V
Gate to source charge	Q _{gs}	—	2	—	nC	V _{GS} = 10 V
Gate to drain charge	Q _{gd}	—	8	—	nC	I _D = 3.5 A
Body to drain diode forward voltage	V _{DF}	—	0.85	1.3	V	I _F = 3.5 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	280	—	ns	I _F = 3.5 A, V _{GS} = 0
Body to drain diode reverse recovery charge	Q _{rr}	—	0.8	—	µC	di _F /dt = 100 A/µs

Note: 4. Pulse test

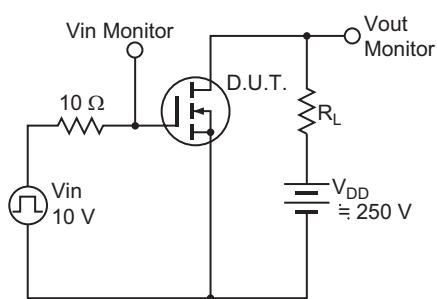
Main Characteristics



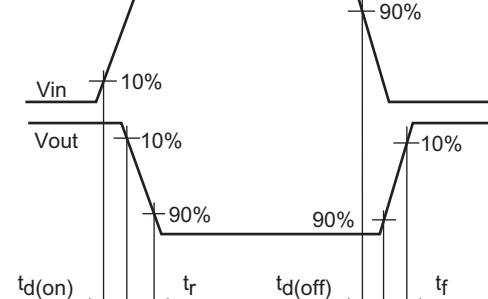




Switching Time Test Circuit



Switching Time Waveform



Package Dimensions

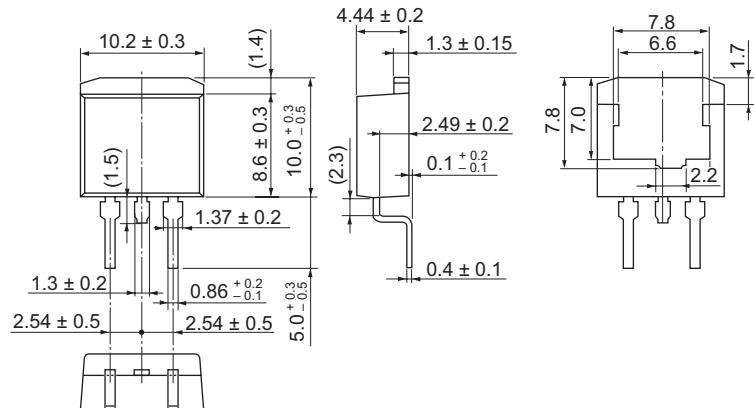
Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
LDPAK(L)	—	PRSS0004AE-A	LDPAK(L) / LDPAK(L)V	1.40g	

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
LDPAK(S)-(1)	SC-83	PRSS0004AE-B	LDPAK(S)-(1) / LDPAK(S)-(1)V	1.30g	

H5N5006LD, H5N5006LS, H5N5006LM

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDPAK(S)-(2)	—	PRSS0004AE-C	LDPAK(S)-(2) / LDPAK(S)-(2)V	1.35g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
H5N5006LD-E	500 pcs	Box (Conductive Sack)
H5N5006LSTL-E	1000 pcs	Taping
H5N5006LMTL-E	1000 pcs	Taping

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