

RJL5012DPP-M0

Silicon N Channel MOS FET
High Speed Power Switching

R07DS0419EJ0100

Rev.1.00

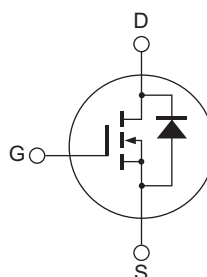
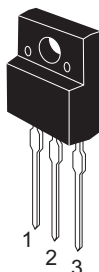
May 26, 2011

Features

- Built-in fast recovery diode
- Low on-resistance
 $R_{DS(on)} = 0.56 \Omega$ typ. (at $I_D = 6 A$, $V_{GS} = 10 V$, $T_a = 25^\circ C$)
- Low leakage current
- High speed switching

Outline

RENESAS Package code: PRSS0003AF-A
(Package name: TO-220FL)



1. Gate
2. Drain
3. Source

Absolute Maximum Ratings

($T_a = 25^\circ C$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D ^{Note4}	12	A
Drain peak current	I_D (pulse) ^{Note1}	36	A
Body-drain diode reverse drain current	I_{DR}	12	A
Body-drain diode reverse drain peak current	I_{DR} (pulse) ^{Note1}	36	A
Avalanche current	I_{AP} ^{Note3}	3	A
Avalanche energy	E_{AR} ^{Note3}	0.5	mJ
Channel dissipation	P_{ch} ^{Note2}	30	W
Channel to case thermal impedance	θ_{ch-c}	4.17	$^\circ C/W$
Channel temperature	T_{ch}	150	$^\circ C$
Storage temperature	T_{stg}	-55 to +150	$^\circ C$

- Notes:
1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. $ST_{ch} = 25^\circ C$, $T_{ch} \leq 150^\circ C$
 4. Limited by maximum safe operation area

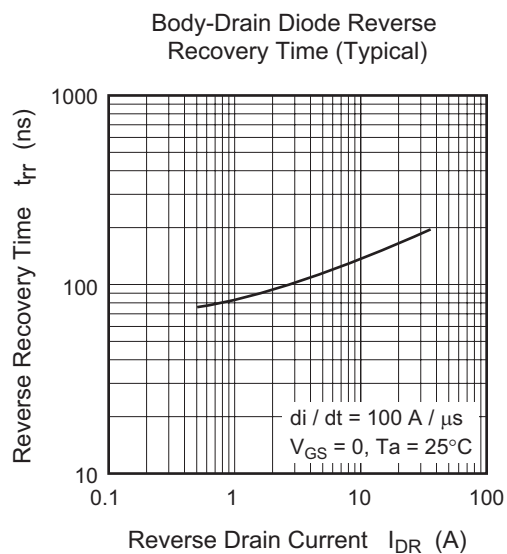
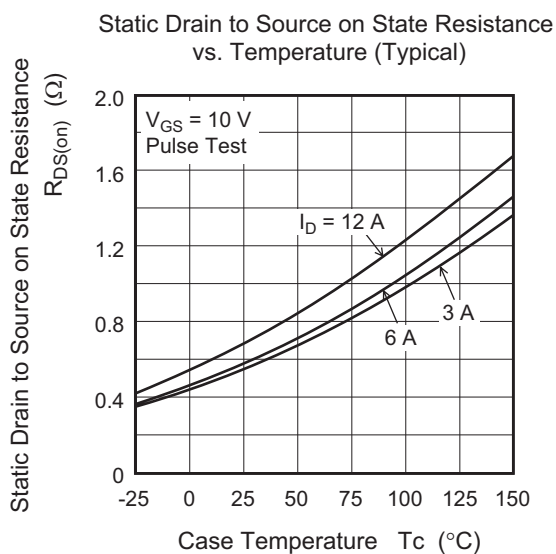
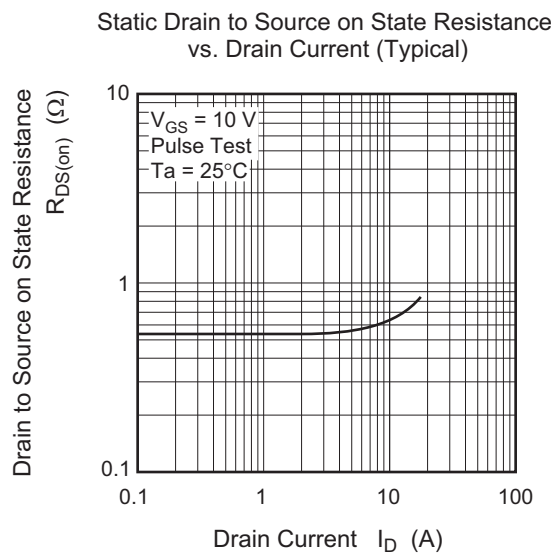
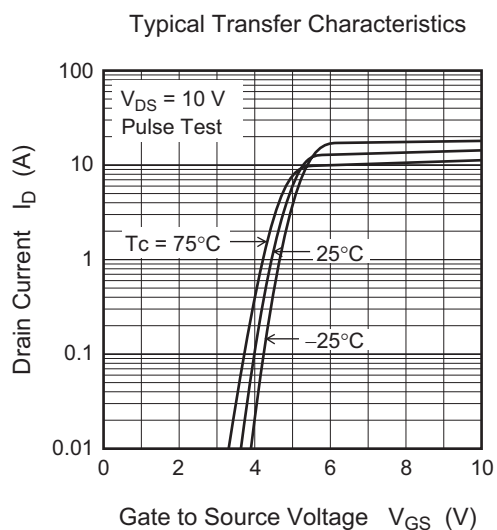
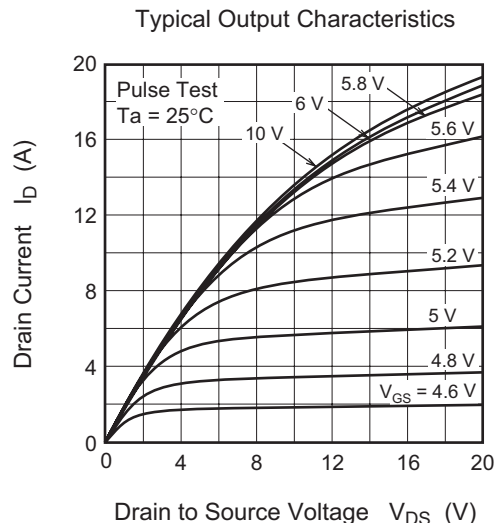
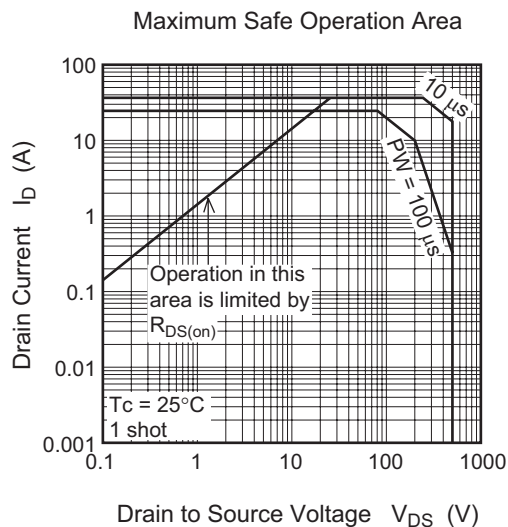
Electrical Characteristics

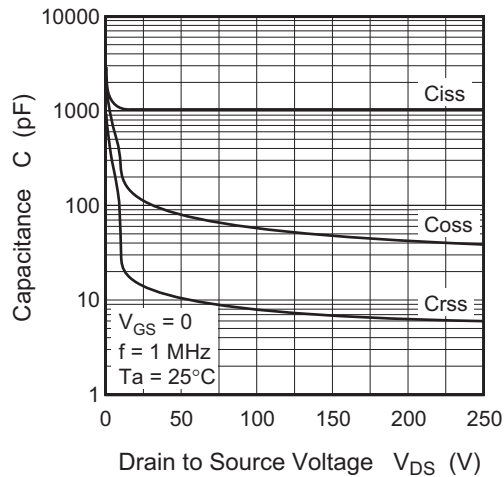
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.56	0.70	Ω	$I_D = 6 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note5}
Input capacitance	C_{iss}	—	1050	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	115	—	pF	
Reverse transfer capacitance	C_{rss}	—	14	—	pF	
Turn-on delay time	$t_{d(on)}$	—	27	—	ns	$I_D = 6 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 41.7 \Omega$ $R_g = 10 \Omega$
Rise time	t_r	—	22	—	ns	
Turn-off delay time	$t_{d(off)}$	—	78	—	ns	
Fall time	t_f	—	15	—	ns	
Total gate charge	Q_g	—	27.8	—	nC	$V_{DD} = 400 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 12 \text{ A}$
Gate to source charge	Q_{gs}	—	4.9	—	nC	
Gate to drain charge	Q_{gd}	—	14.4	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.96	1.60	V	$I_F = 12 \text{ A}$, $V_{GS} = 0$ ^{Note5}
Body-drain diode reverse recovery time	t_{rr}	—	140	—	ns	$I_F = 12 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

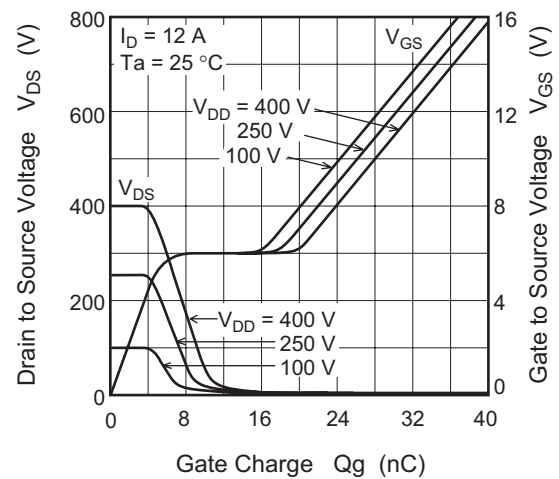
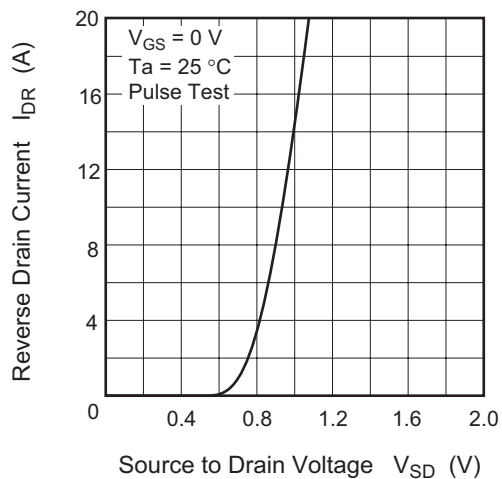
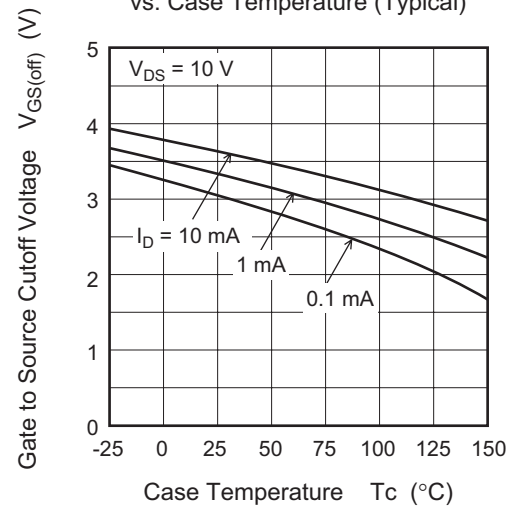
Notes: 5. Pulse test

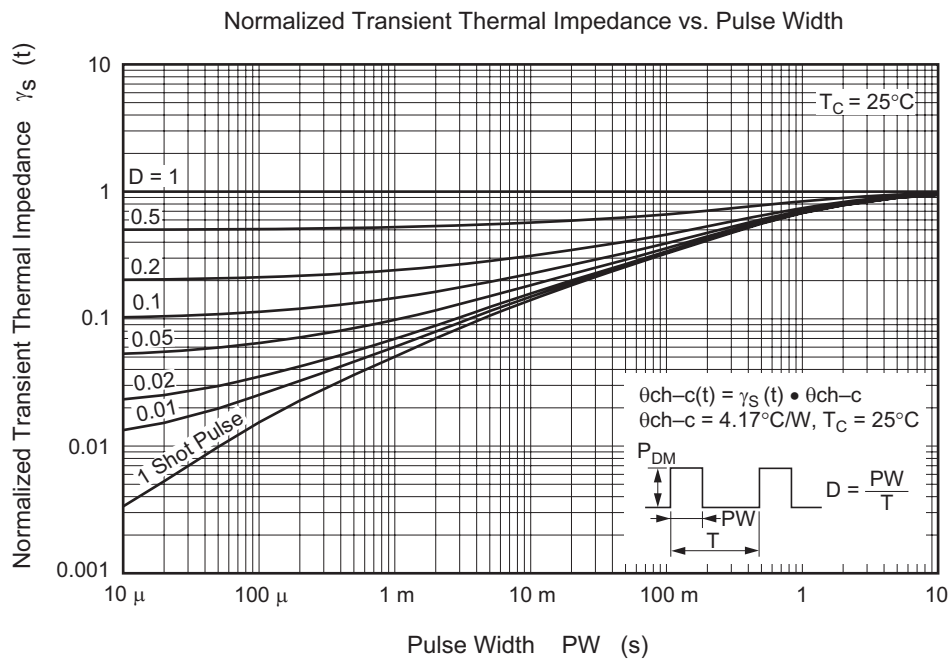
Main Characteristics



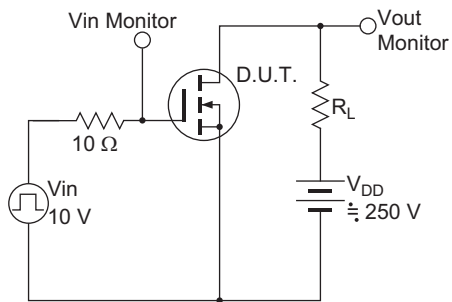
Typical Capacitance vs.
Drain to Source Voltage

Dynamic Input Characteristics (Typical)

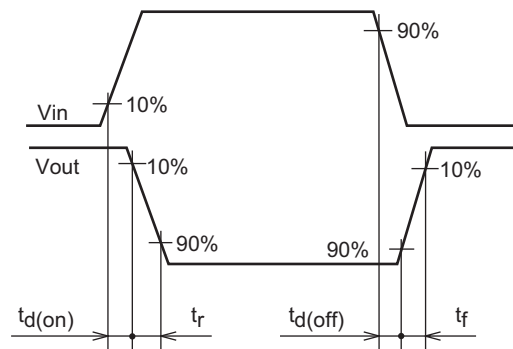
Reverse Drain Current vs.
Source to Drain Voltage (Typical)Gate to Source Cutoff Voltage
vs. Case Temperature (Typical)



Switching Time Test Circuit



Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
TO-220FL	—	PRSS0003AF-A	TO-220FL	1.5g	

The drawing shows the mechanical dimensions of the RJL5012DPP-M0 package. The top view shows a square body with a width of 10.0 ± 0.3 mm and a height of 15.0 ± 0.3 mm. The mounting holes are spaced 3.0 ± 0.3 mm apart. The central hole has a diameter of $\phi 3.2 \pm 0.2$ mm. The side view shows a total height of 12.5 ± 0.5 mm, with a mounting tab height of 3.6 ± 0.3 mm. The mounting tab has a width of 2.54 ± 0.25 mm. The lead height is 1.15 ± 0.2 mm, and the lead thickness is 0.75 ± 0.15 mm. The lead length is 2.54 ± 0.25 mm. The lead width is 0.40 ± 0.15 mm. The detail view shows a lead width of 2.6 ± 0.2 mm and a lead thickness of 4.5 ± 0.2 mm.

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJL5012DPP-M0-T2	600 pcs	Box (Tube)

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Laviel' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141