



STB4N62K3 STD4N62K3

N-channel 620 V, 1.7 Ω , 3.8 A SuperMESH3™ Power MOSFET
DPAK, D²PAK

Features

Order codes	V _{DSS}	R _{DS(on)} max	I _D	P _w
STB4N62K3 STD4N62K3	620 V	< 2 Ω	3.8 A	70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Application

Switching applications

Description

These devices are made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

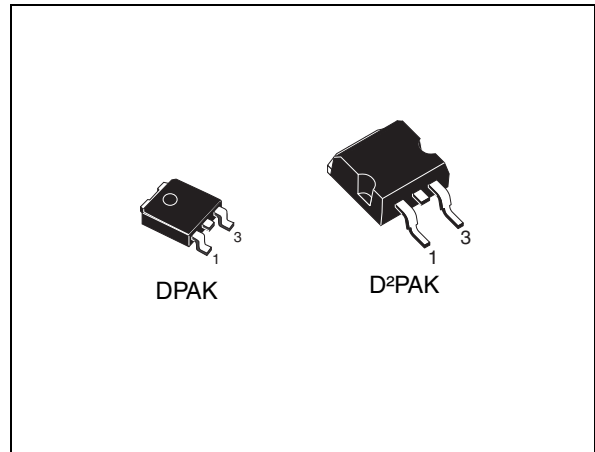


Figure 1. Internal schematic diagram

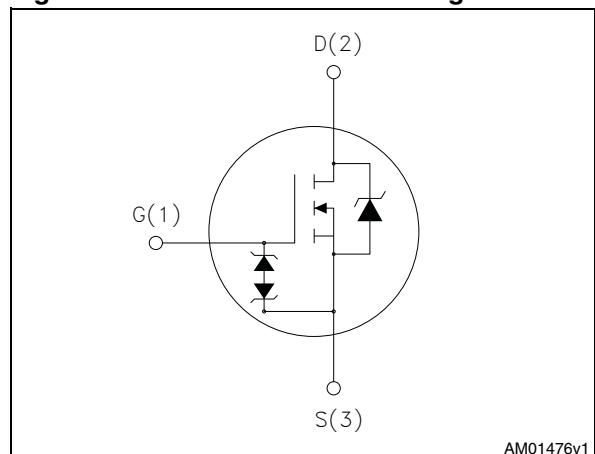


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB4N62K3 STD4N62K3	4N62K3	D ² PAK DPAK	Tape and reel

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 9

4 **Package mechanical data** 10

5 **Revision history** 18



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK	DPAK	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	620		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	3.8		A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	2		A
$I_{DM}^{(1)}$	Drain current (pulsed)	15.2		A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	70		W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	3.8		A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	115		mJ
$V_{ESD(G-S)}$	Gate source ESD(HBM-C = 100 pF, $R = 1.5\text{ k}\Omega$)	2500		V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	12		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)			V
T_{stg}	Storage temperature	- 55 to 150		$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 3.8\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	D ² PAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.79		$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	30	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	620			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.9\text{ A}$		1.7	2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	550 42 7	-	pF pF pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }496\text{ V}$, $V_{GS} = 0$	-	27	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 496\text{ V}$, $I_D = 3.8\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 18)	-	22 4 13	-	nC nC nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 1.9\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17)	-	10	-	ns
t_r	Rise time			9		ns
$t_{d(off)}$	Turn-off-delay time			29		ns
t_f	Fall time			19		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		3.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				15.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3.8\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 3.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 22)	-	220		ns
Q_{rr}	Reverse recovery charge			1.4		μC
I_{RRM}	Reverse recovery current			13		A
t_{rr}	Reverse recovery time	$I_{SD} = 3.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 22)	-	270		ns
Q_{rr}	Reverse recovery charge			1.9		μC
I_{RRM}	Reverse recovery current			14		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

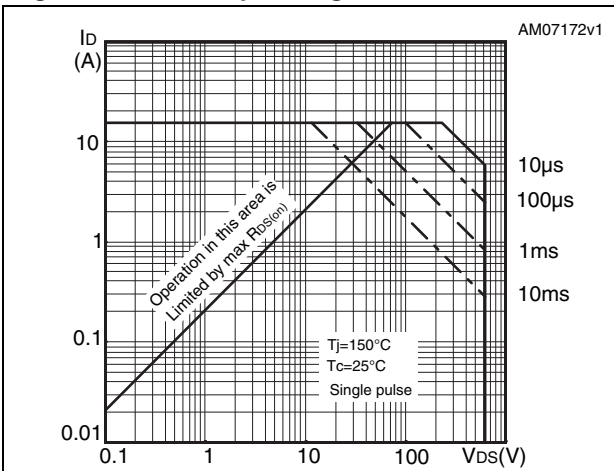


Figure 3. Thermal impedance for D²PAK

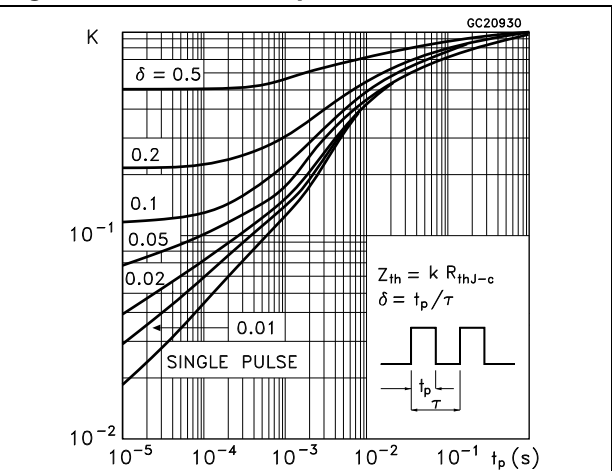


Figure 4. Safe operating area for DPAK

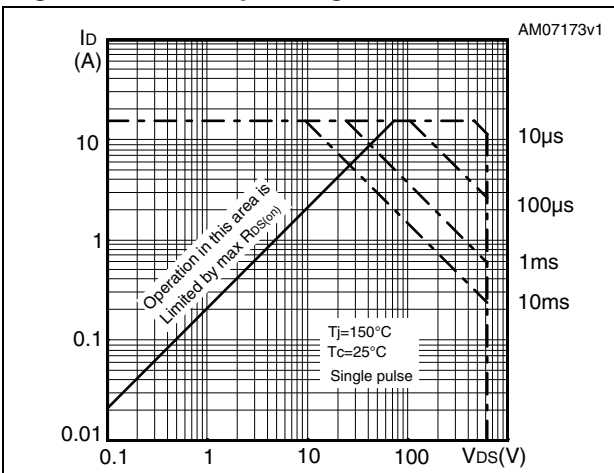


Figure 5. Thermal impedance for DPAK

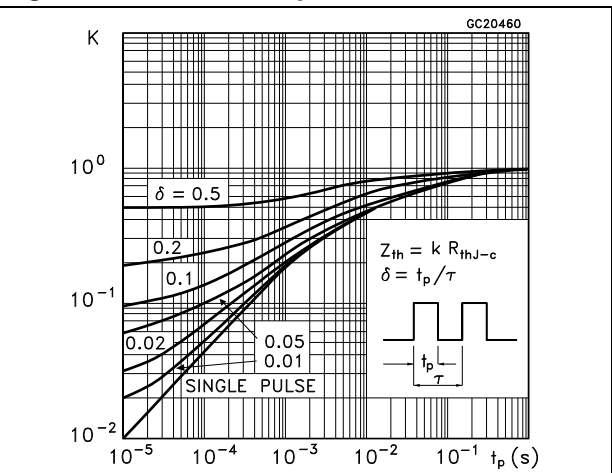


Figure 6. Output characteristics

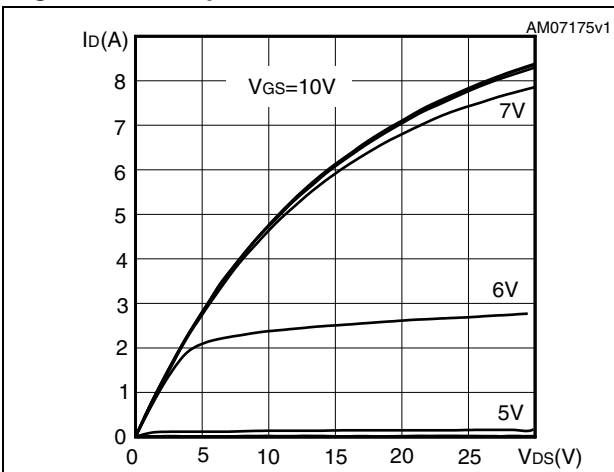


Figure 7. Transfer characteristics

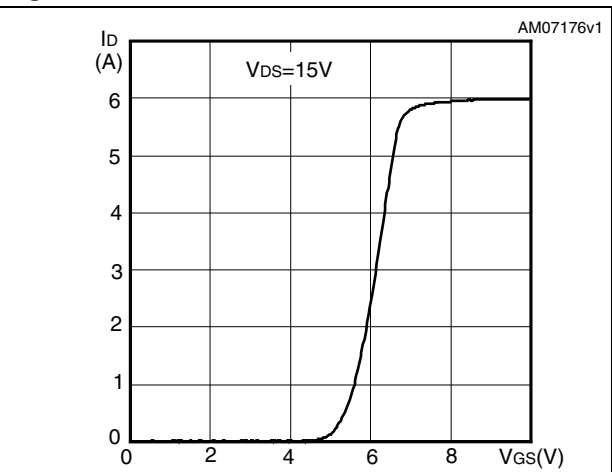


Figure 8. Gate charge vs gate-source voltage Figure 9. Static drain-source on resistance

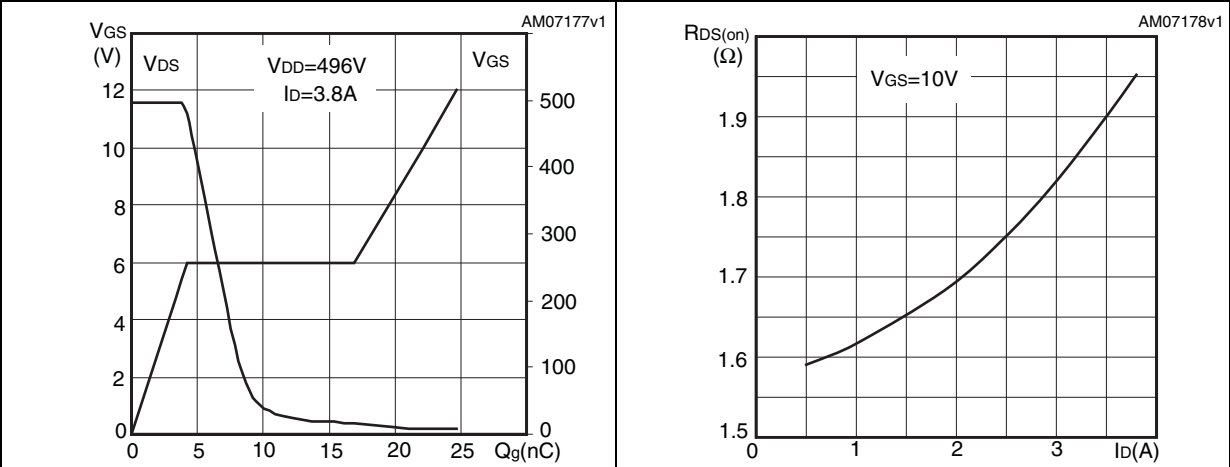


Figure 10. Capacitance variations Figure 11. Output capacitance stored energy

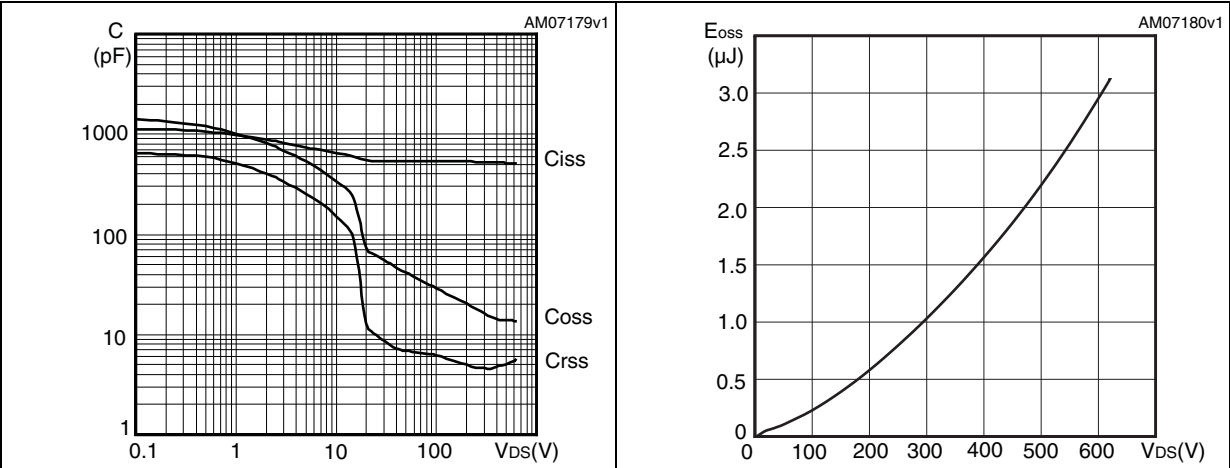


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized on resistance vs temperature

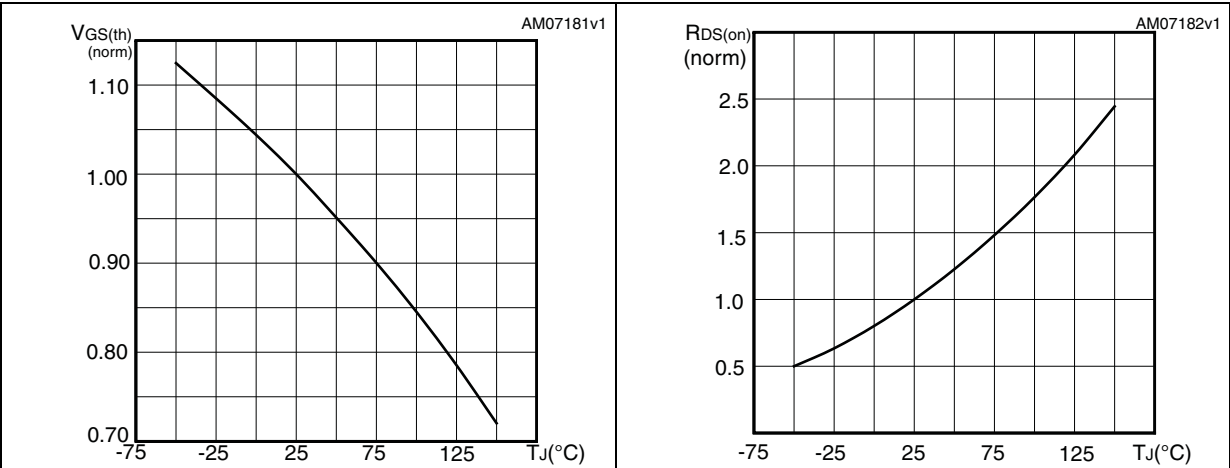


Figure 14. Maximum avalanche energy vs starting T_J

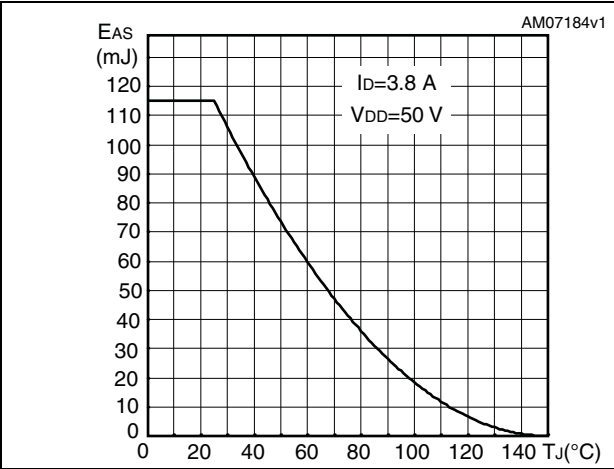


Figure 15. Normalized B_{VDSS} vs temperature

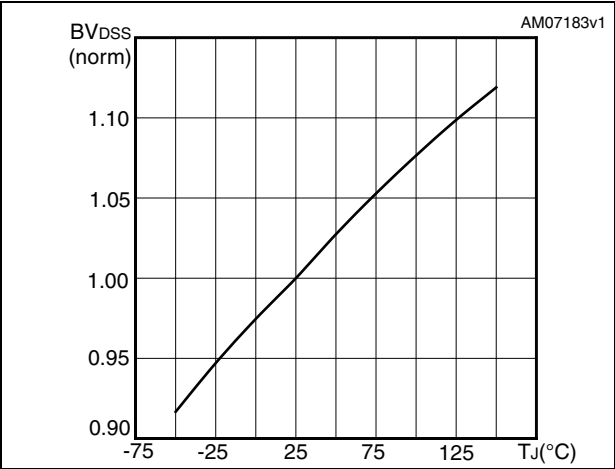
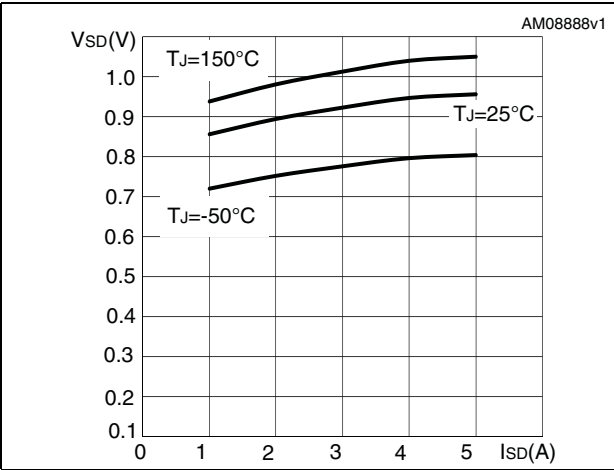


Figure 16. Source-drain diode forward characteristics



3 Test circuits

Figure 17. Switching times test circuit for resistive load

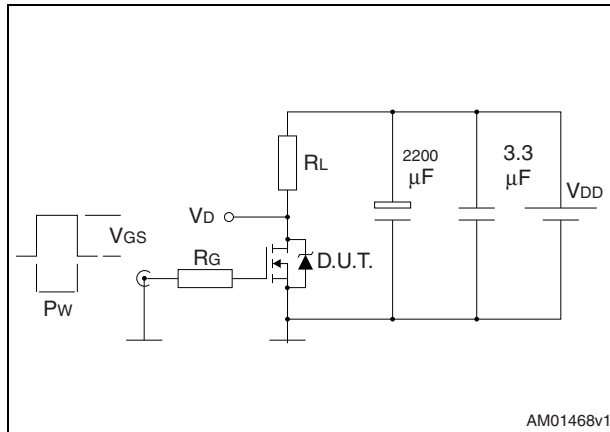


Figure 18. Gate charge test circuit



Figure 19. Test circuit for inductive load switching and diode recovery times

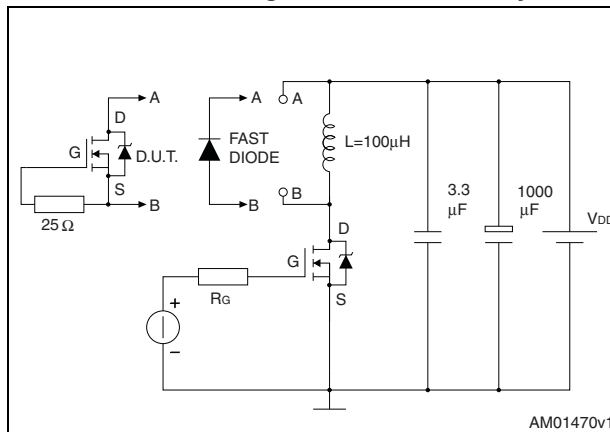


Figure 20. Unclamped Inductive load test circuit



Figure 21. Unclamped inductive waveform

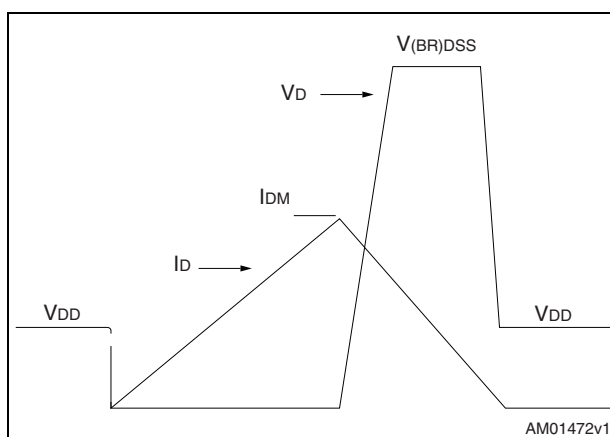
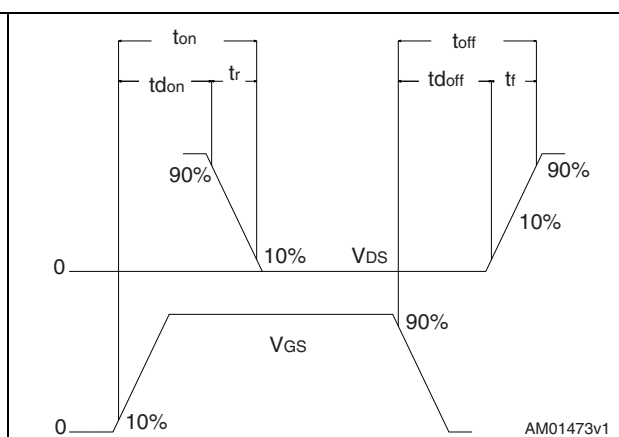


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 23. DPAK (TO-252) drawing

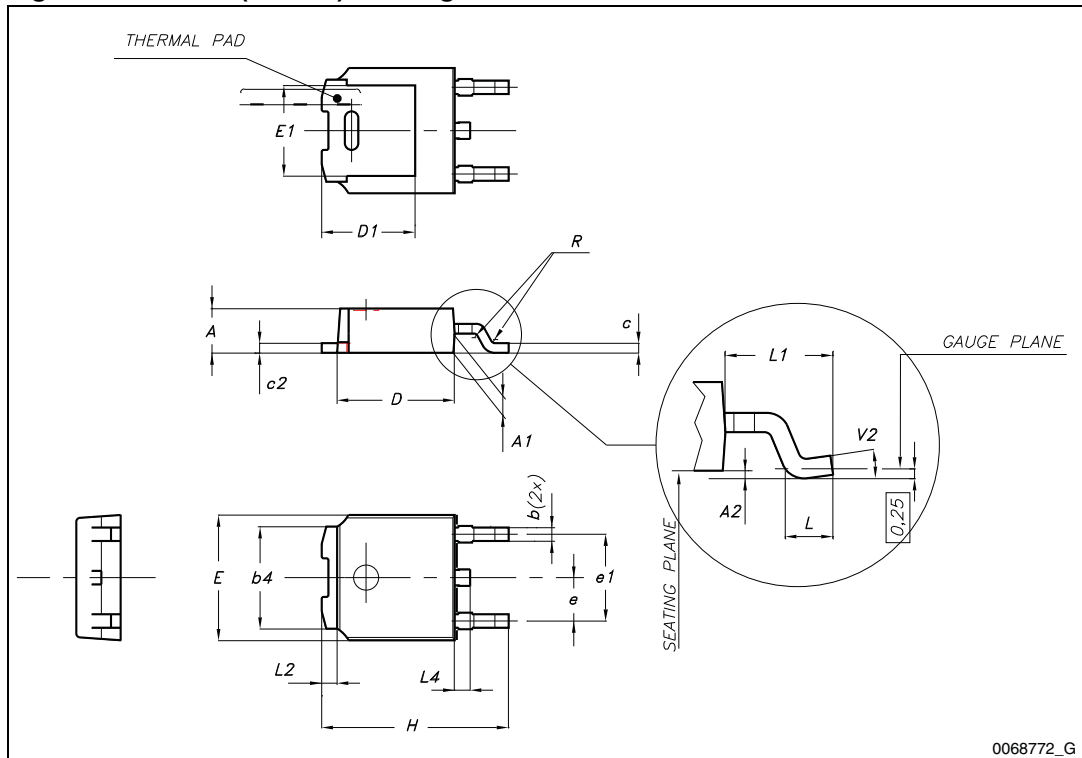
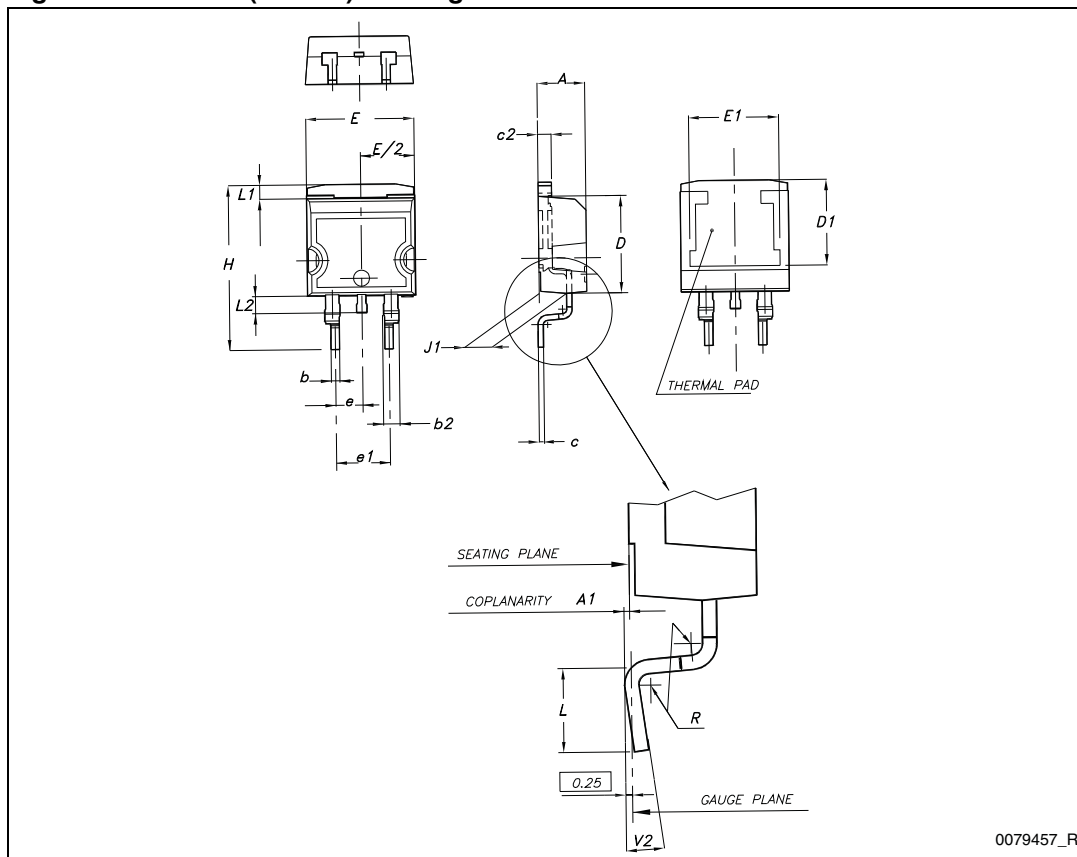


Table 10. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

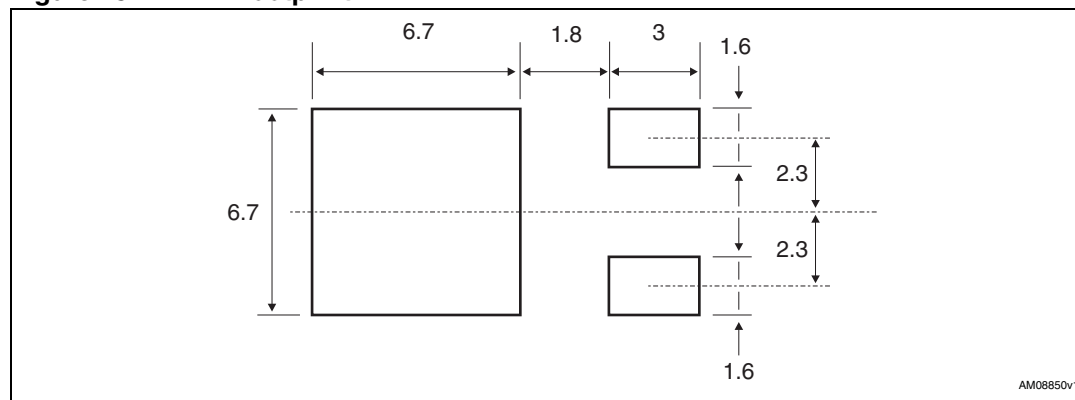
Figure 24. D²PAK (TO-263) drawing

0079457_R

Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 25. DPAK footprint^(a)

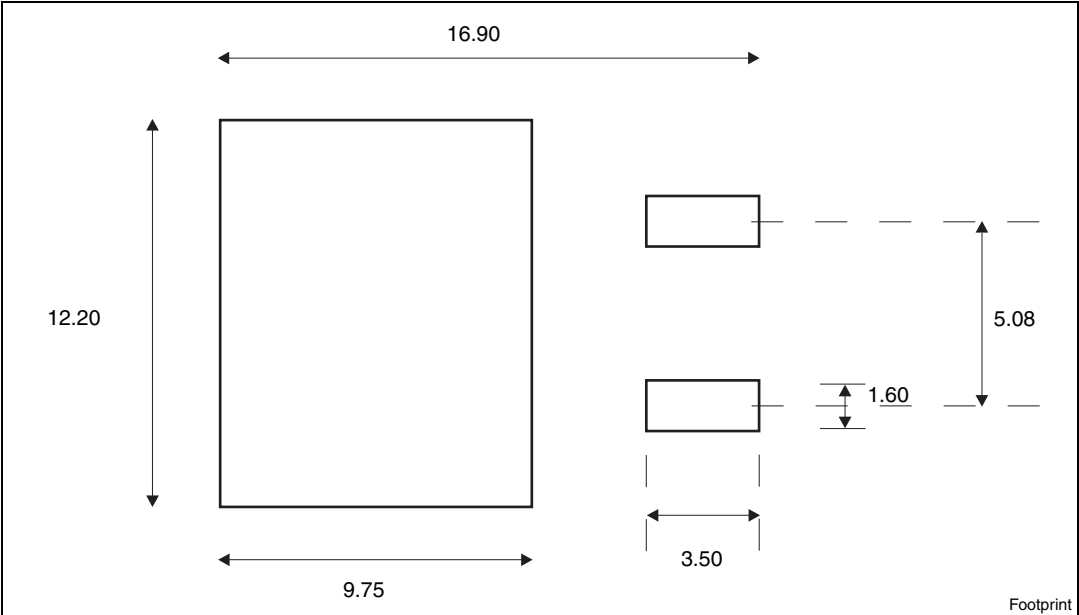


a. All dimension are in millimeters

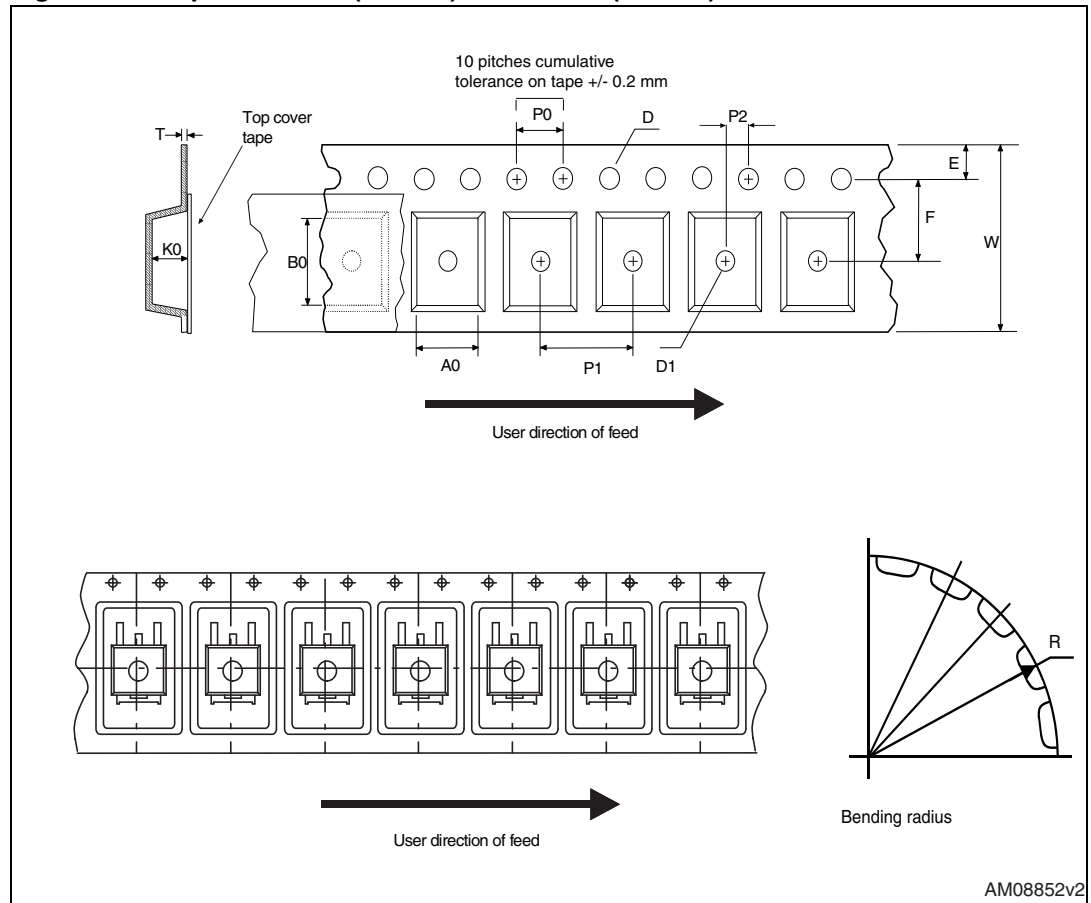
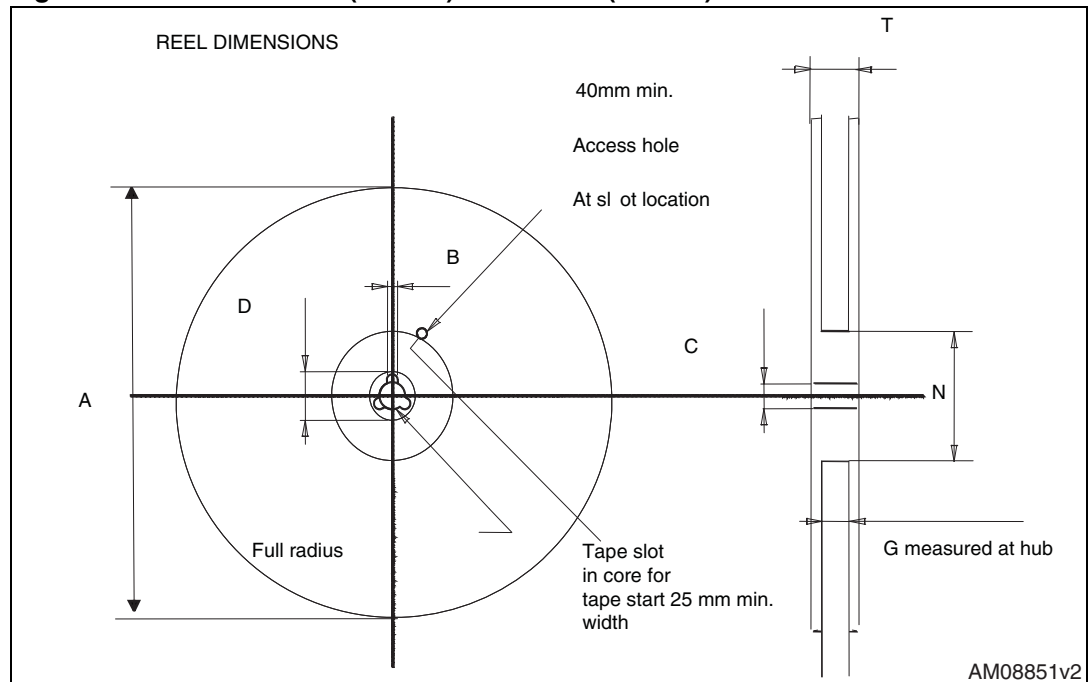
Table 12. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 26. D²PAK footprint^(b)



b. All dimension are in millimeters

Figure 27. Tape for DPAK (TO-252) and D²PAK (TO-263)Figure 28. Reel for DPAK (TO-252) and D²PAK (TO-263)

5 Revision history

Table 13. Document revision history

Date	Revision	Changes
16-Dec-2010	1	First release

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2010 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

