



# STD4NK100Z

N-channel 1000 V, 5.6  $\Omega$ , 2.2 A SuperMESH™ Power MOSFET  
Zener-protected in DPAK package

Datasheet — preliminary data

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD4NK100Z	1000 V	< 6.8 $\Omega$	2.2 A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Very good manufacturing repeatability

## Applications

- Switching application
  - Automotive

## Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

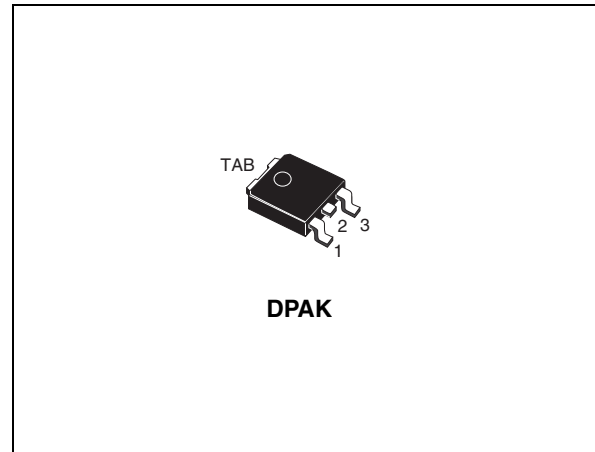


Figure 1. Internal schematic diagram

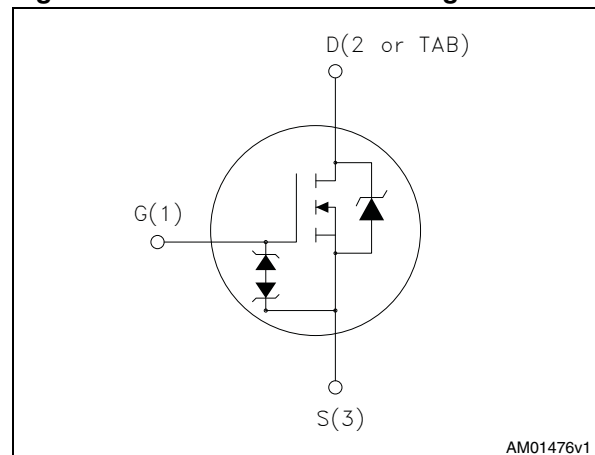


Table 1. Device summary

Order code	Marking	Package	Packaging
STD4NK100Z	4NK100Z	DPAK	Tape and reel

Contents

1      **Electrical ratings** ..... 3

2      **Electrical characteristics** ..... 4

3      **Test circuits** ..... 6

4      **Package mechanical data** ..... 7

5      **Packaging mechanical data** ..... 9

6      **Revision history** ..... 11



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	1000	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	2.2	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1	A
$I_{DM}^{(1)}$	Drain current (pulsed)	8.8	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	90	W
	Derating factor	0.72	W/ $^{\circ}\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100pF, R=1.5 k $\Omega$ )	3000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	TBD	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 2.2\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.39	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{JMAX}$ )	2.2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	TBD	mJ

## 2 Electrical characteristics

( $T_{CASE}=25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	1000			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 1000\text{ V}$ , $V_{DS} = 1000\text{ V}$ , $T_c = 125\text{ }^{\circ}\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{GS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1.1\text{ A}$		5.6	6.8	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS}=25\text{ V}$ , $f=1\text{ MHz}$ , $V_{GS}=0$	-	601	-	pF
$C_{oss}$	Output capacitance			53		pF
$C_{rss}$	Reverse transfer capacitance			12		pF
$C_{oss,eq}^{(1)}$	Equivalent output capacitance	$V_{GS}=0$ , $V_{DS}=0\text{ V to }800\text{ V}$	-	TBD	-	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD}=500\text{ V}$ , $I_D=1.25\text{ A}$ , $R_G=4.7\text{ }\Omega$ , $V_{GS}=10\text{ V}$ (see <a href="#">Figure 4</a> )	-	15	-	ns
$t_r$	Rise time			7.5		ns
$t_{d(off)}$	Off-voltage rise time			32		ns
$t_f$	Fall time			39		ns
$Q_g$	Total gate charge	$V_{DD}=800\text{ V}$ , $I_D=2.5\text{ A}$	-	18	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS}=10\text{ V}$		3.6		nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 3</a> )		9.2		nC

1.  $C_{oss,eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		2.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.2 \text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 2.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 100 \text{ V}$ (see <a href="#">Figure 2</a> )	-	584 2.3 8		ns $\mu\text{C}$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 2.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 100 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 2</a> )	-	628 2.5 8.1		ns $\mu\text{C}$ A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

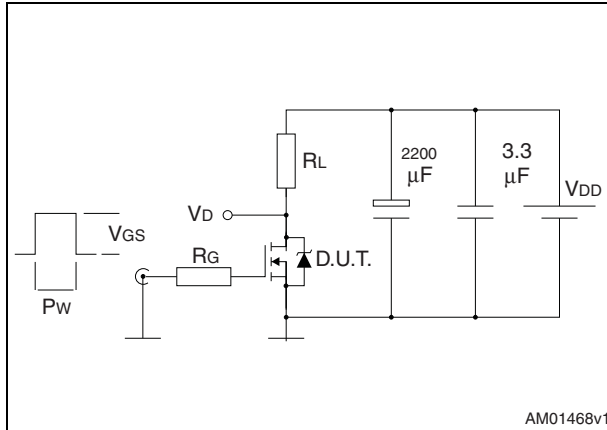
**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{gs} = \pm 1 \text{ mA}$ (open drain)	30		-	V

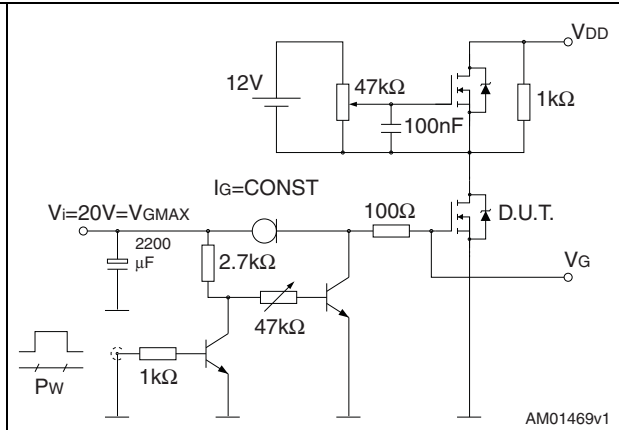
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

### 3 Test circuits

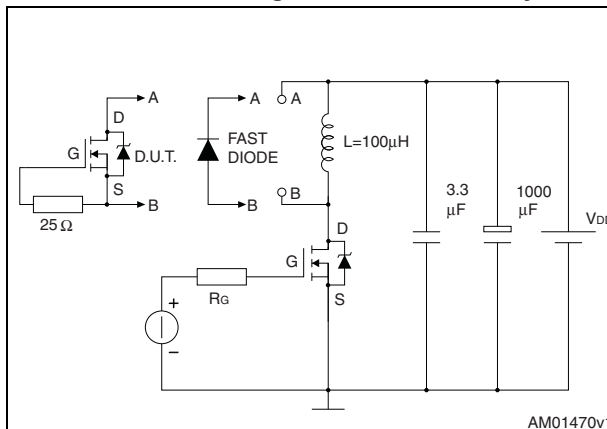
**Figure 2. Switching times test circuit for resistive load**



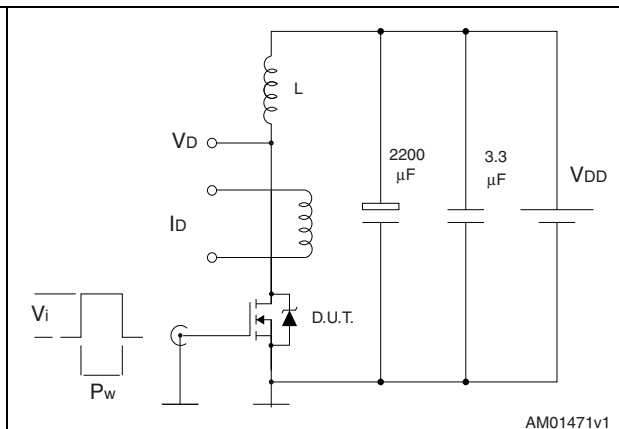
**Figure 3. Gate charge test circuit**



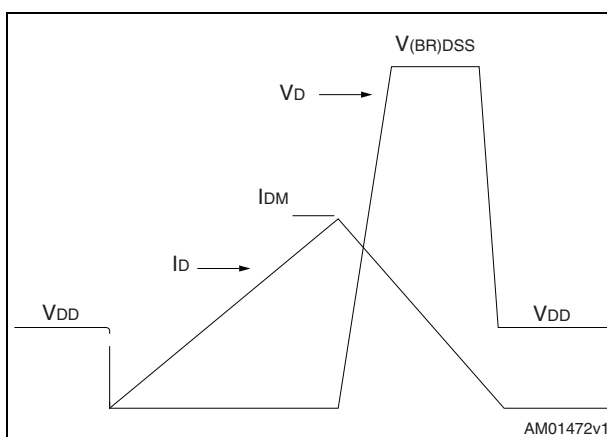
**Figure 4. Test circuit for inductive load switching and diode recovery times**



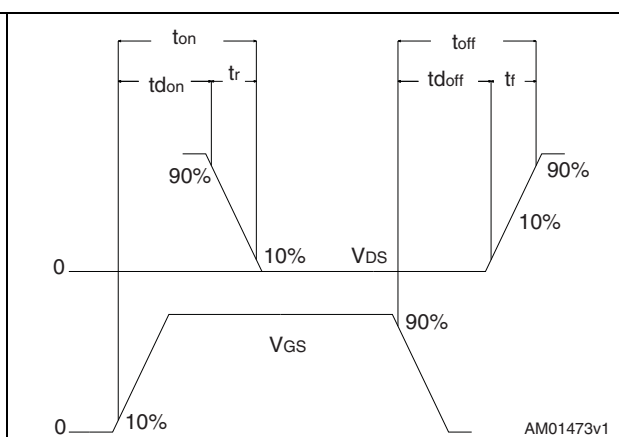
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9. DPAK (TO-252) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 8. DPAK (TO-252) drawing

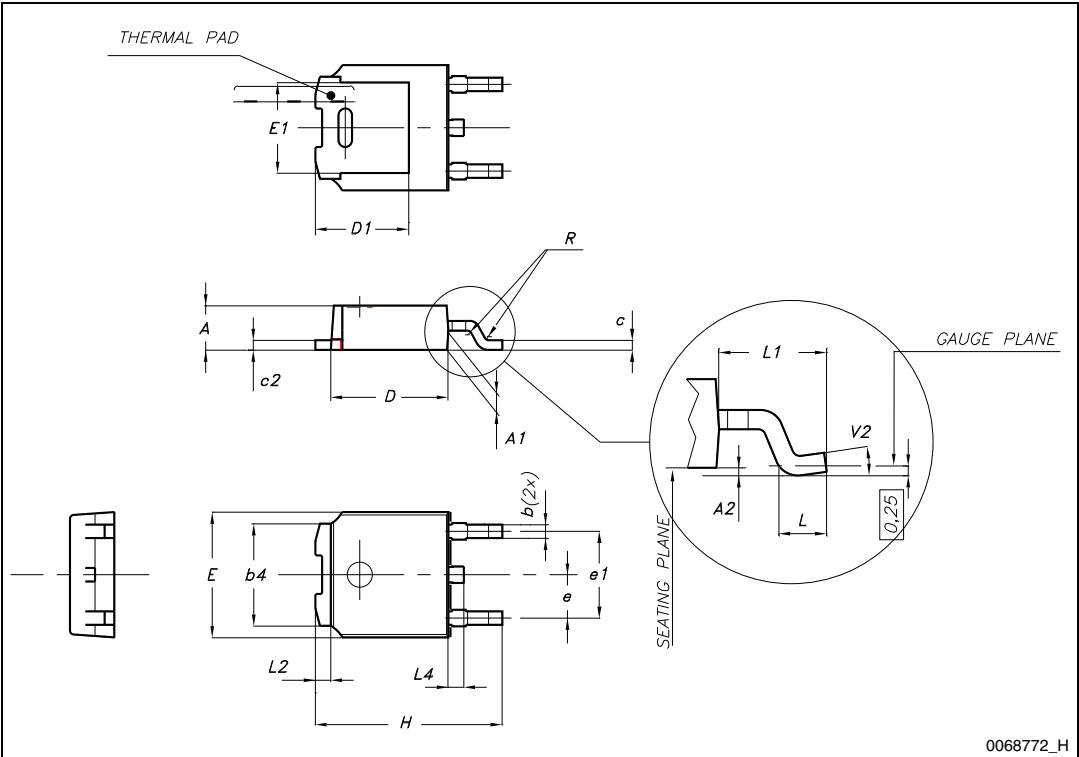
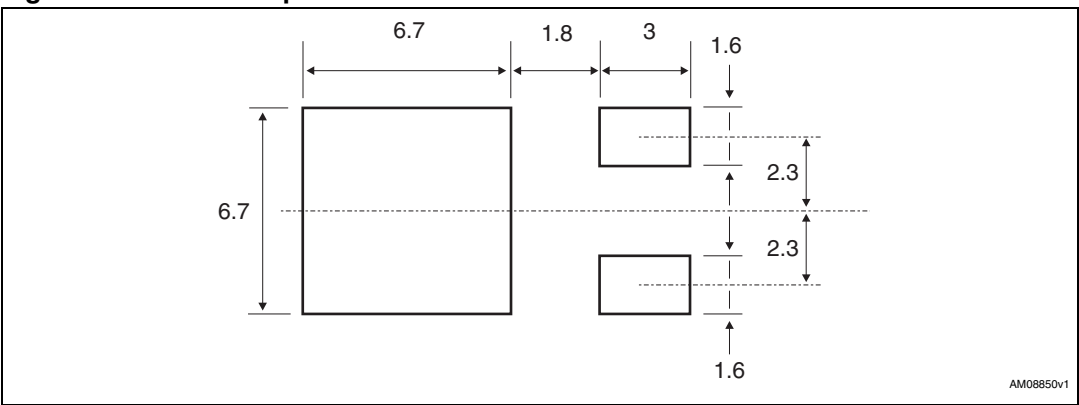


Figure 9. DPAK footprint<sup>(a)</sup>



a. All dimensions are in millimeters



## 5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 10. Tape for DPAK (TO-252)

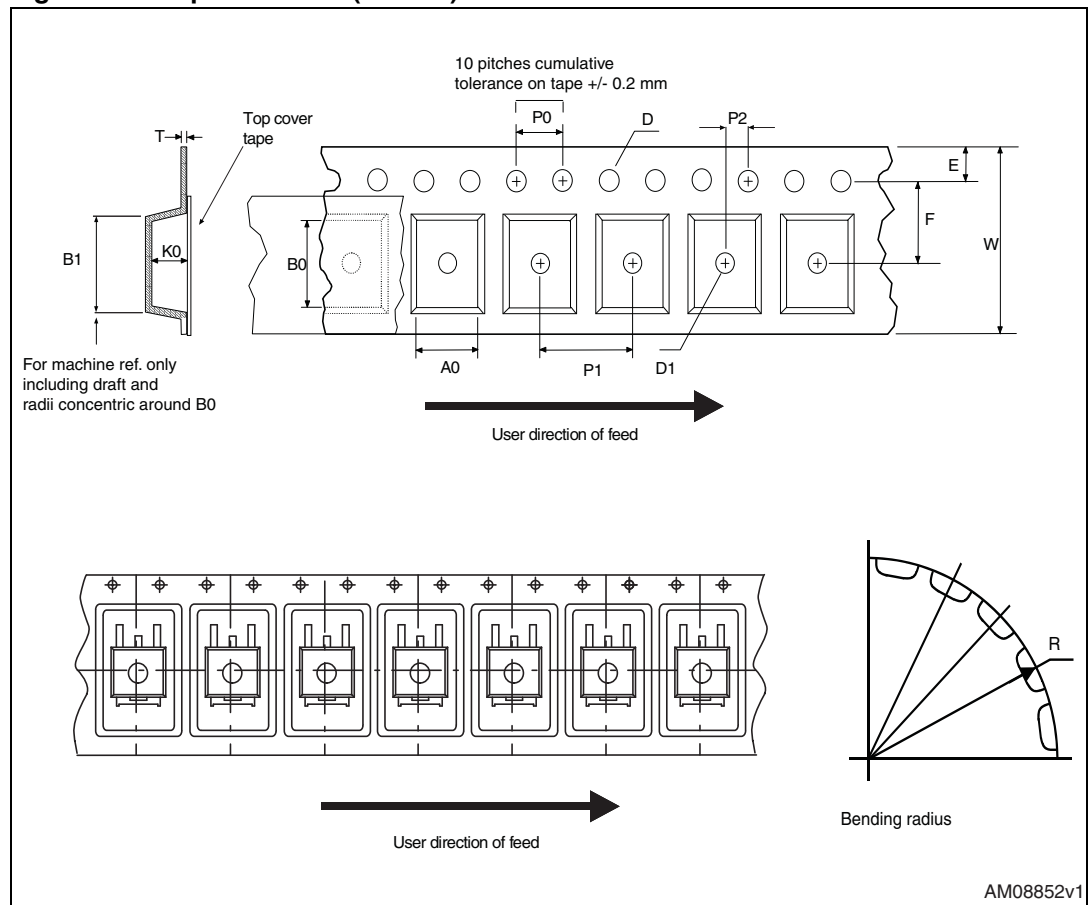
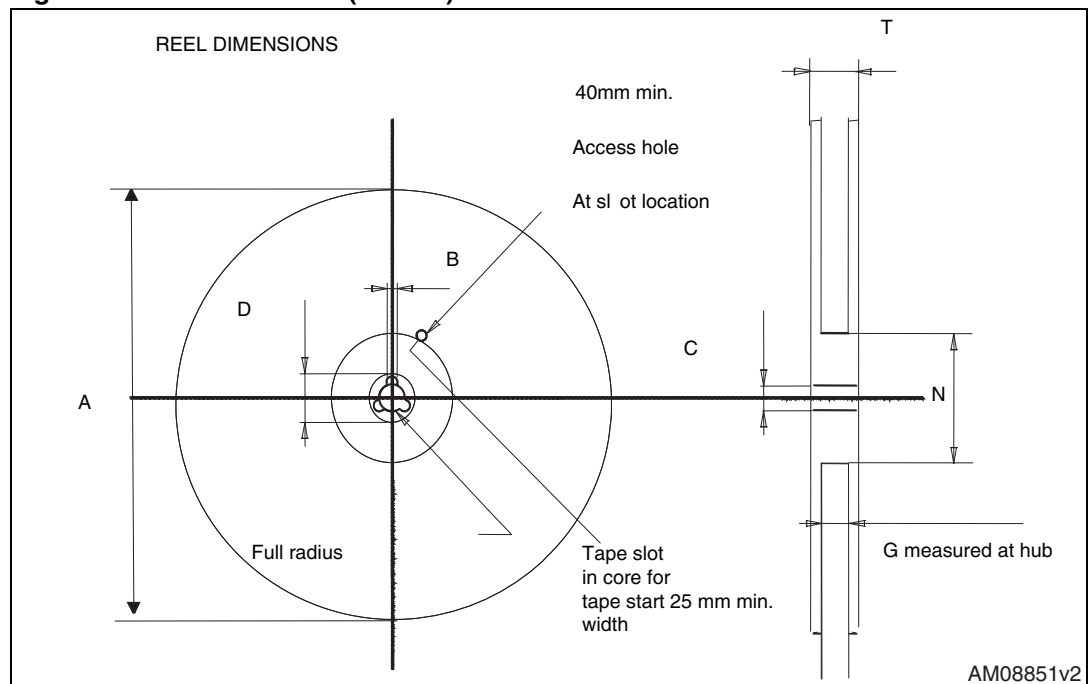


Figure 11. Reel for DPAK (TO-252)



## 6 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
02-mar-2012	1	First release.

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