



N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16406Q3

FEATURES

- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

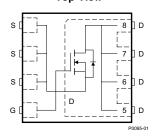
APPLICATIONS

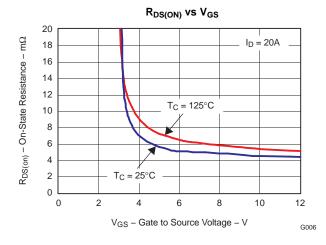
- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control or Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.







PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage		V	
Q_g	Gate Charge Total (4.5V) 5.8			nC
Q_{gd}	Gate Charge Gate to Drain	1.5		nC
Б	Design to Course On Design	V _{GS} = 4.5V	5.9	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10V	4.2	mΩ
V_{th}	Threshold Voltage	1.8		V

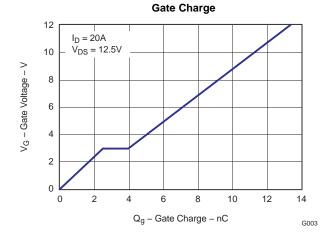
ORDERING INFORMATION

Device	Package	Media	Qty	Ship	
CSD16406Q3	SON 3.3 × 3.3 Plastic Package	13-inch reel	2500	Tape and Reel	

ABSOLUTE MAXIMUM RATINGS

T _A = 2	5°C unless otherwise stated	VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	٧
V_{GS}	Gate to Source Voltage	+16 / -12	٧
	Continuous Drain Current, T _C = 25°C	60	Α
I _D	Continuous Drain Current ⁽¹⁾	19	Α
I_{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	114	Α
P_D	Power Dissipation ⁽¹⁾	2.7	W
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I_D = 45A, L = 0.1mH, R_G = 25 Ω	101	mJ

- (1) $R_{\theta JA} = 46^{\circ}\text{C/W}$ on 1in^2 Cu (2 oz.) on 0.060" thick FR4 PCB.
- (2) Pulse width ≤300µs, duty cycle ≤2%





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Cl	haracteristics	•				
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +16/-12V$			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.4	1.8	2.2	V
D	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 20A$		5.9	7.4	mΩ
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = 10V, I_D = 20A$		4.2	5.3	mΩ
g _{fs}	Transconductance	$V_{DS} = 15V, I_D = 20A$			S	
Dynamic	Characteristics					
C _{ISS}	Input Capacitance			840	1100	pF
Coss	Output Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz$		680	950	pF
C _{RSS}	Reverse Transfer Capacitance			57	80	pF
R _g	Series Gate Resistance			1.2	2.4	Ω
Q _g	Gate Charge Total (4.5V)			5.8	8.1	nC
Q _{gd}	Gate Charge Gate to Drain	V 42.5V L 20A		1.5		nC
Q _{gs}	Gate Charge Gate to Source	V _{DS} = 12.5V, I _D = 20A		2.5		nC
Qg(th)	Gate Charge at Vth			1.5		nC
Q _{OSS}	Output Charge	V _{DS} = 13.6V, V _{GS} = 0V		13.9		nC
t _{d(on)}	Turn On Delay Time			7.3		ns
t _r	Rise Time	$V_{DS} = 13.6V, V_{GS} = 0V$ $V_{DS} = 12.5V, V_{GS} = 4.5V I_{D} = 20A$ $R_{G} = 2\Omega$		12.9		ns
t _{d(off)}	Turn Off Delay Time	$R_G = 2\Omega$		8.5		ns
t _f	Fall Time			4.8		ns
Diode C	haracteristics					
V_{SD}	Diode Forward Voltage	$I_{S} = 20A, V_{GS} = 0V$		0.85	1.0	V
Q _{rr}	Reverse Recovery Charge	$V_{DD} = 13.6V$, $I_F = 20A$, $di/dt = 300A/\mu s$		18		nC
t _{rr}	Reverse Recovery Time	$V_{DD} = 13.6V$, $I_F = 20A$, $di/dt = 300A/\mu s$		22		ns
	•	•				

THERMAL CHARACTERISTICS

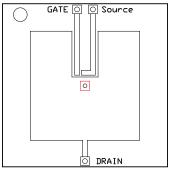
 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	MIN	TYP	MAX	TINU
R $_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			2.7	°C/W
R $_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾ (2)			58	°C/W

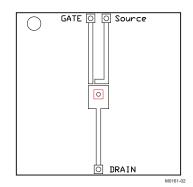
⁽¹⁾ $R_{\theta JC}$ is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 x 1.5 in 0.06 inch thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 Material with 1 inch² of 2 oz. Cu.





Max $R_{\theta JA} = 58^{\circ} C/W$ when mounted on 1 inch² of 2 oz. Cu.



Max $R_{\theta JA} = 162^{\circ}C/W$ when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

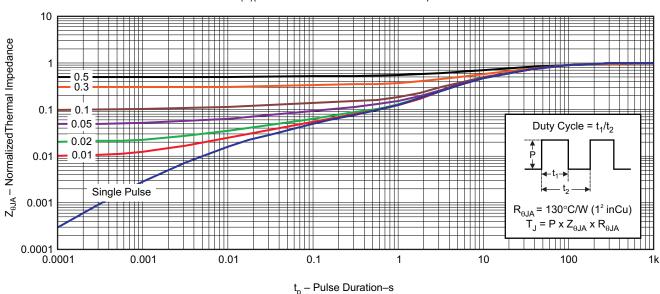


Figure 1. Transient Thermal Impedance

G012



TYPICAL MOSFET CHARACTERISTICS (continued)

$(T_A = 25^{\circ}C \text{ unless otherwise stated})$

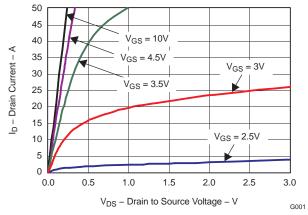


Figure 2. Saturation Characteristics

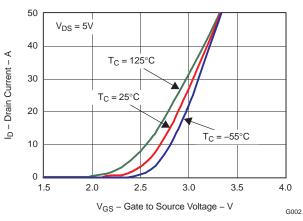


Figure 3. Transfer Characteristics

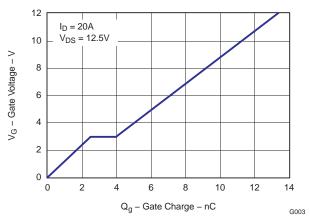


Figure 4. Gate Charge

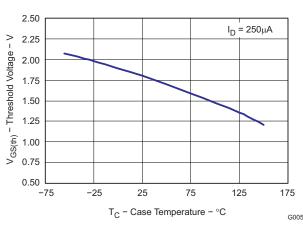


Figure 6. Threshold Voltage vs. Temperature

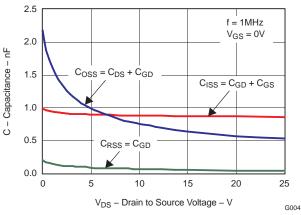


Figure 5. Capacitance

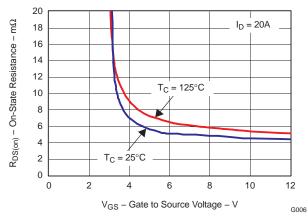


Figure 7. On Resistance vs. Gate Voltage



TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

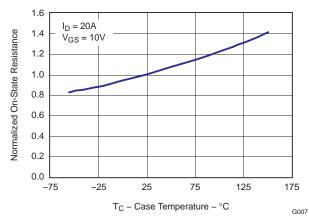


Figure 8. Normalized On Resistance vs. Temperature

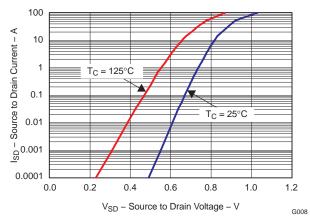


Figure 9. Typical Diode Forward Voltage

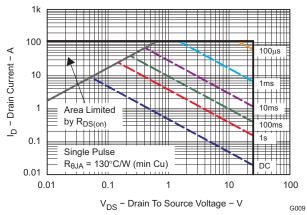


Figure 10. Maximum Safe Operating Area

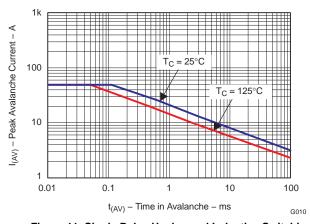


Figure 11. Single Pulse Unclamped Inductive Switching

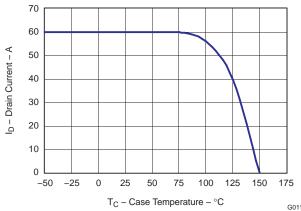
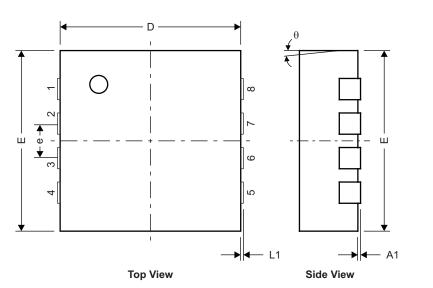


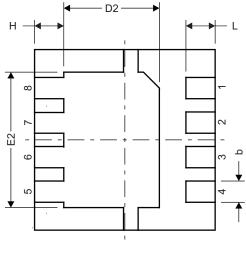
Figure 12. Maximum Drain Current vs. Temperature



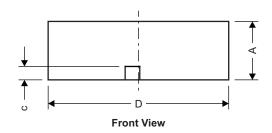
MECHANICAL DATA

Q3 Package Dimensions





Bottom View

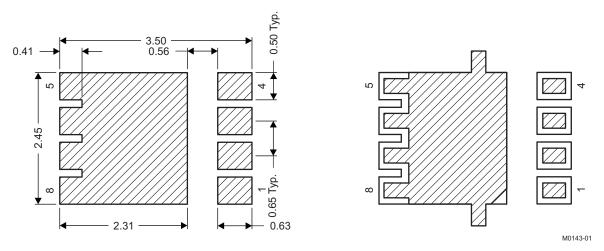


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DIM	MILLIMETERS				INCHES	
	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
С	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	-	-	-	_	-	_
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	-	-	-	_	-	_
E2	2.350	2.450	2.550	0.093	0.096	0.100
е		0.650 TYP			0.026	
Н	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	-	-	_			
θ	_	_	_	_	_	_

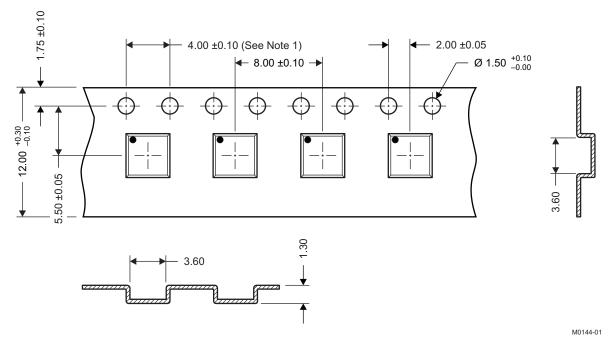


Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

Q3 Tape and Reel Information



Notes:

- 1. 10 sprocket hole pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- 3. Material:black static dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified)
- 5. Thickness: 0.30 ±0.05mm
- 6. MSL1 260°C (IR and Convection) PbF Reflow Compatible



REVISION HISTORY

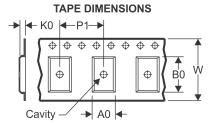
Cł	changes from Original (August 2009) to Revision A	Page
•	Deleted the Package Marking Information section	

PACKAGE MATERIALS INFORMATION

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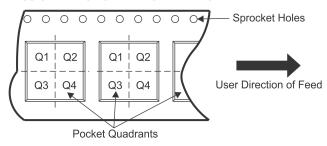
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

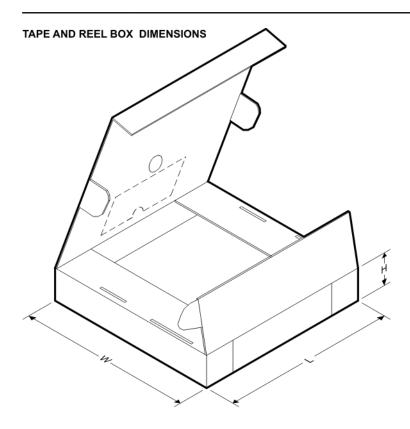
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16406Q3	VSON- CLIP	DQG	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1

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*All dimensions are nominal

Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16406Q3	VSON-CLIP	DQG	8	2500	336.6	336.6	41.3

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