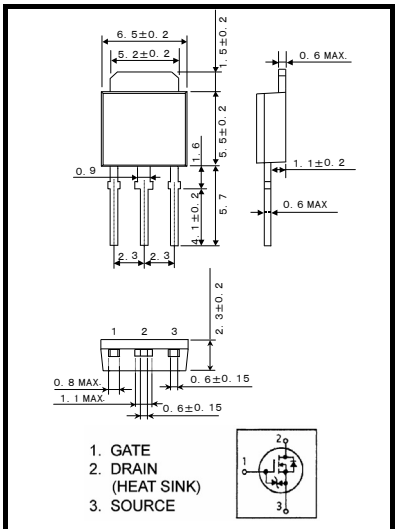
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type ($L^2-\pi-$MOS V)

2SK4019

Chopper Regulator, DC/DC Converter and Motor Drive Applications

- 4 V gate drive
- Low drain−source ON-resistance : $R_{DS\ (ON)}$ = 0.17 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 4.5 S (typ.)
- Low leakage current : I_{DSS} = 100 μA (max) (V_{DS} = 100 V)
- Enhancement mode : V_{th} = 0.8~2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-7J2B

Weight: 0.36 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	100	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	5	A
	Pulse (Note 1)	I_{DP}	20	A
Drain power dissipation (Tc = 25°C)		P_D	20	W
Single-pulse avalanche energy (Note 2)		E_{AS}	180	mJ
Avalanche current		I_{AR}	5	A
Repetitive avalanche energy (Note 3)		E_{AR}	2	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	6.25	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	125	°C / W

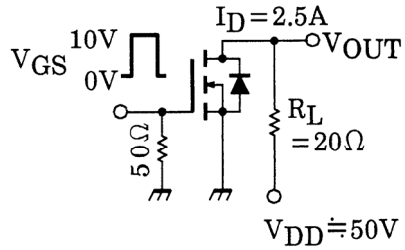
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 25 V, T_{ch} = 25°C (initial), L = 11.6 mH, R_G = 25 Ω, I_{AR} = 5 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Handle with care.

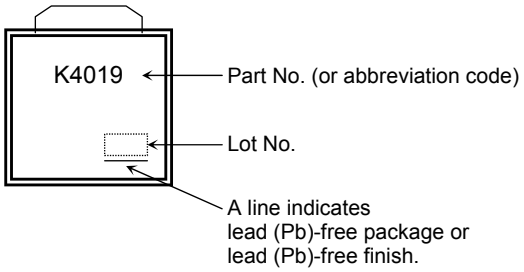
Electrical Characteristics (Ta = 25°C)

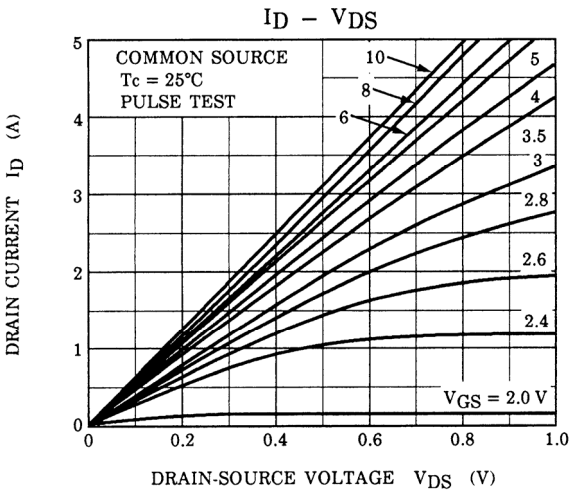
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cutoff current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain−source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 2.5 A	—	0.22	0.30	Ω
			V_{GS} = 10 V, I_D = 2.5 A	—	0.17	0.23	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 2.5 A	2.0	4.5	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	500	—	pF
Reverse transfer capacitance		C_{rss}		—	80	—	
Output capacitance		C_{oss}		—	190	—	
Switching time	Rise time	t_r		—	17	—	ns
	Turn−on time	t_{on}		—	25	—	
	Fall time	t_f		—	50	—	
	Turn−off time	t_{off}		—	195	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≒ 80 V, V_{GS} = 10 V, I_D = 5 A	—	22	—	nC
Gate−source charge		Q_{gs}		—	15	—	
Gate−drain (“Miller”) charge		Q_{gd}		—	7	—	

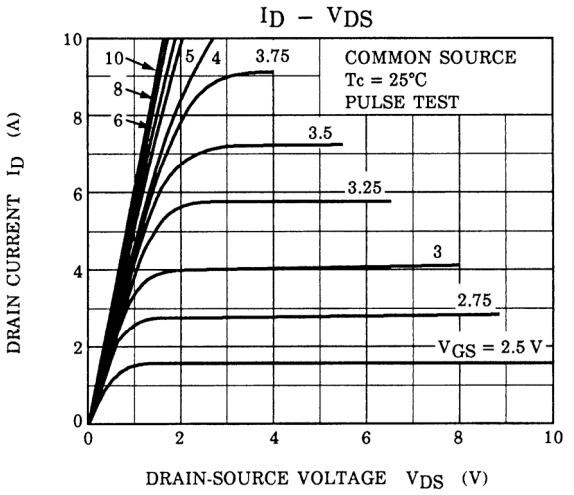
Source−Drain Ratings and Characteristics (Ta = 25°C)

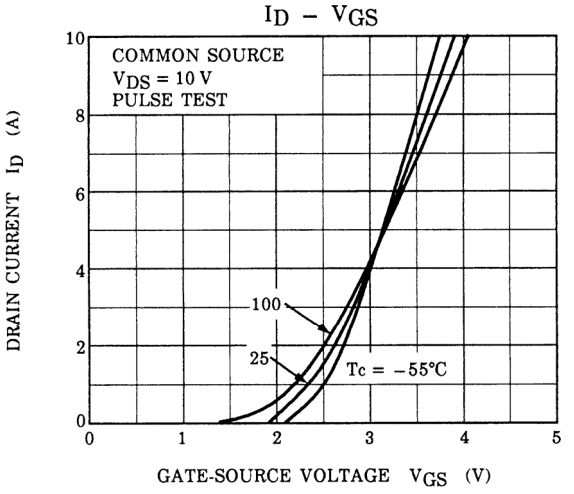
Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	5	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	20	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 5 A, V_{GS} = 0 V	—	—	−1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 5 A, V_{GS} = 0 V, dI_{DR} / dt = 50 A / μs	—	160	—	ns
Reverse recovery charge	Q_{rr}		—	0.28	—	μC

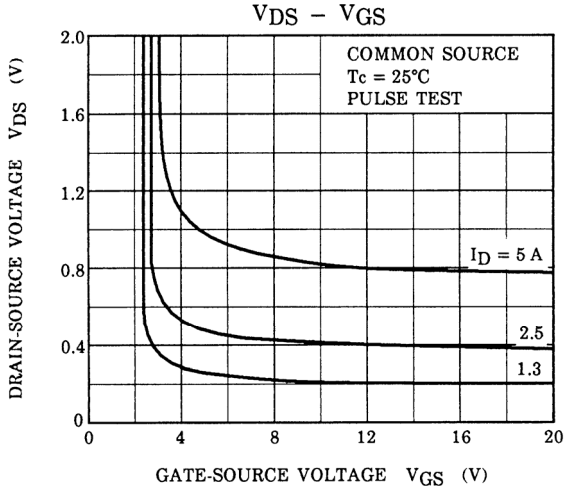
Marking

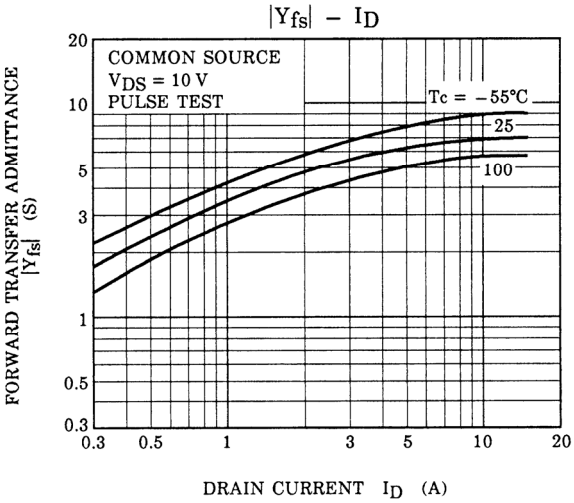


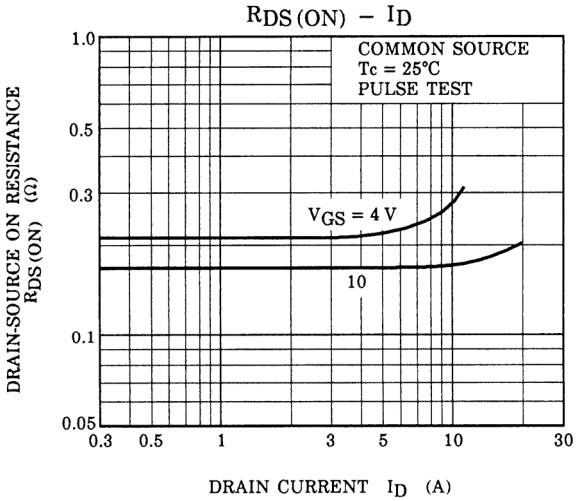

I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
10
8
6
5
4
3.5
3
2.8
2.6
2.4
V_{GS} = 2.0 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)


I_D – V_{DS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
10
8
6
5
4
3.75
3.5
3.25
3
2.75
V_{GS} = 2.5 V
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)

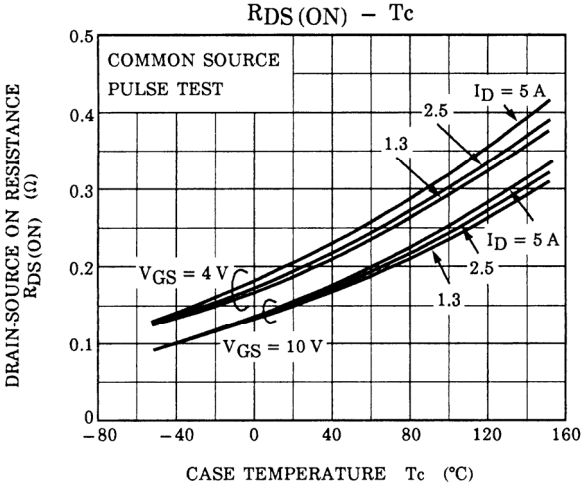

I_D – V_{GS}
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
100
25
Tc = −55°C
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)


V_{DS} – V_{GS}
COMMON SOURCE
Tc = 25°C
PULSE TEST
I_D = 5 A
2.5
1.3
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)

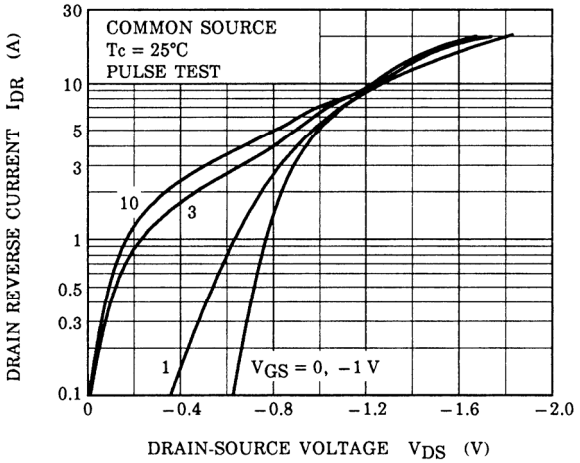

$|Y_{fs}|$ – I_D
COMMON SOURCE
V_{DS} = 10 V
PULSE TEST
Tc = −55°C
25
100
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)


$R_{DS\,(ON)}$ – I_D
COMMON SOURCE
Tc = 25°C
PULSE TEST
V_{GS} = 4 V
10
DRAIN-SOURCE ON RESISTANCE $R_{DS\,(ON)}$ (Ω)
DRAIN CURRENT I_D (A)

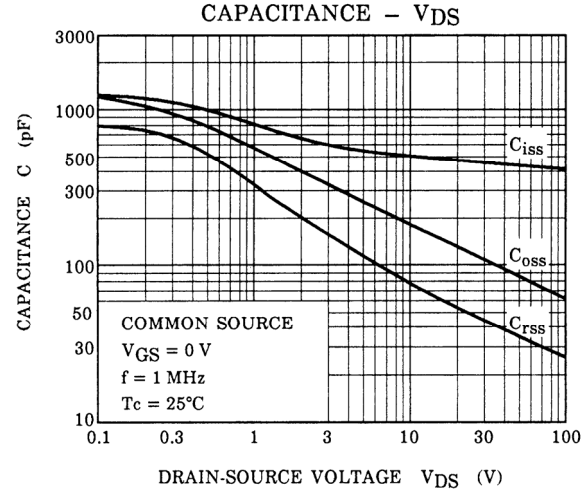
$R_{DS\,(ON)}$ – Tc



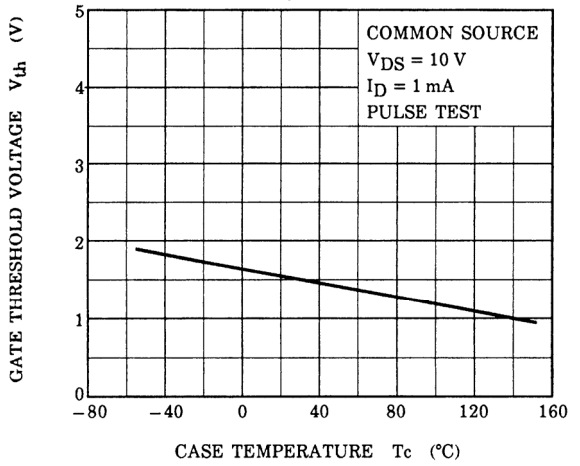
I_{DR} – V_{DS}



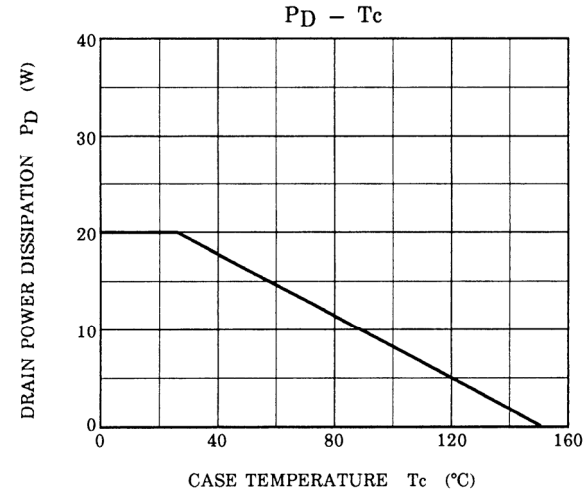
CAPACITANCE – V_{DS}



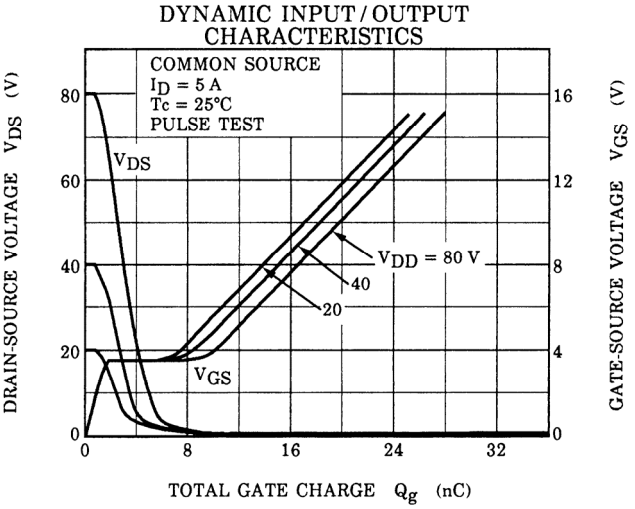
V_{th} – Tc



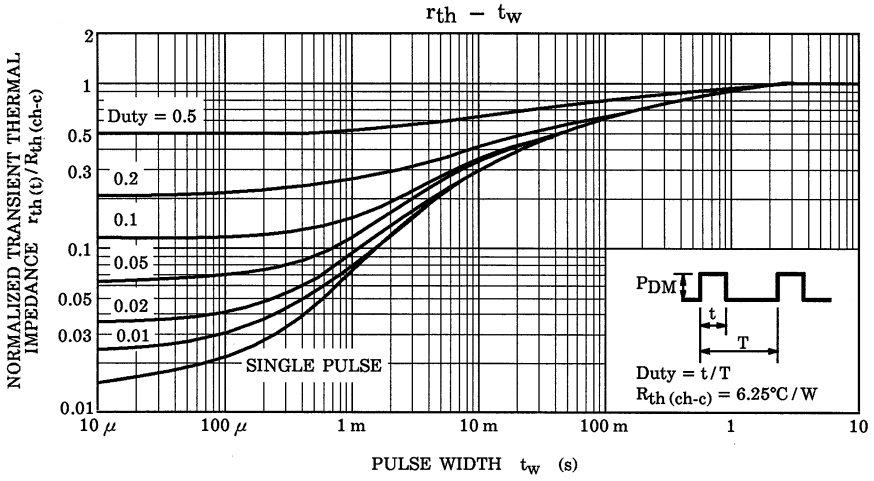
P_D – Tc



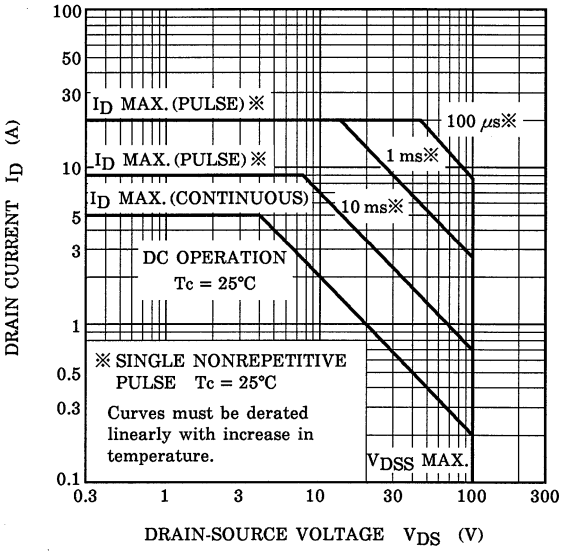
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



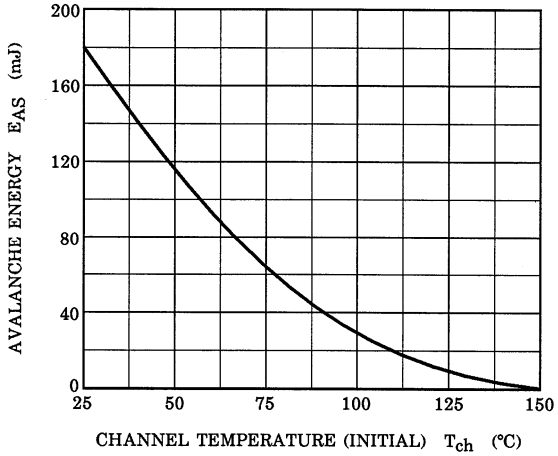
$r_{th} - t_w$

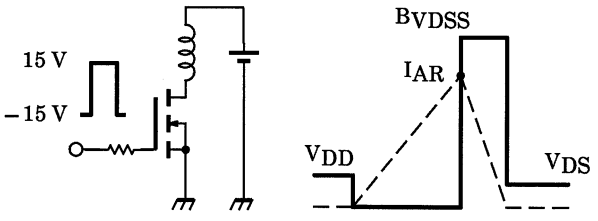


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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