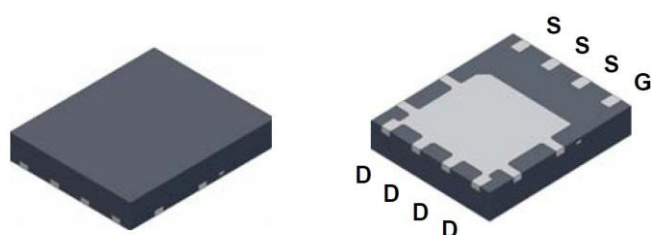


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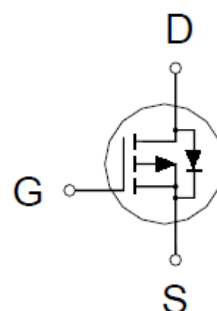
P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	14mΩ @ $V_{GS} = 10V$	-30A



PDFN 5*6P



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ °C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	
Continuous Drain Current	$T_C = 25\text{ °C}$ (Package Limited)	I_D	-30	A
	$T_C = 25\text{ °C}$ (Silicon Limited)		-52	
	$T_C = 100\text{ °C}$		-33	
Pulsed Drain Current ¹		I_{DM}	-150	
Continuous Drain Current	$T_A = 25\text{ °C}$	I_D	-10	
	$T_A = 70\text{ °C}$		-8	
Avalanche Current		I_{AS}	-40	mJ
Avalanche Energy		E_{AS}	83	
Power Dissipation	$T_C = 25\text{ °C}$	P_D	62.5	W
	$T_C = 100\text{ °C}$		25	
	$T_A = 25\text{ °C}$		2.5	
	$T_A = 70\text{ °C}$		1.6	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.6	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 25V$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125^{\circ}C$			10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-150			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -9A$		17	22	m Ω
		$V_{GS} = -10V, I_D = -12A$		11	14	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -12A$		28		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		2200		pF
Output Capacitance	C_{oss}			410		
Reverse Transfer Capacitance	C_{rss}			270		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		4.6		Ω
Total Gate Charge ²	$Q_g(V_{GS} = 10V)$	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = -10V, I_D = -12A$		42		nC
	$Q_g(V_{GS} = 4.5V)$			20		
Gate-Source Charge ²	Q_{gs}			3.5		
Gate-Drain Charge ²	Q_{gd}			6.7		
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = -15V, I_D \cong -2A, V_{GS} = -10V, R_{GS} = 6\Omega$		12		nS
Rise Time ²	t_r			16		
Turn-Off Delay Time ²	$t_{d(off)}$			50		
Fall Time ²	t_f			100		

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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_j = 25 °C)

Continuous Current ³	I _S				-52	A
Forward Voltage ¹	V _{SD}	I _F = -12A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = 12A, dI _F /dt = 100A / μS		22		nS
Reverse Recovery Charge	Q _{rr}			11		nC

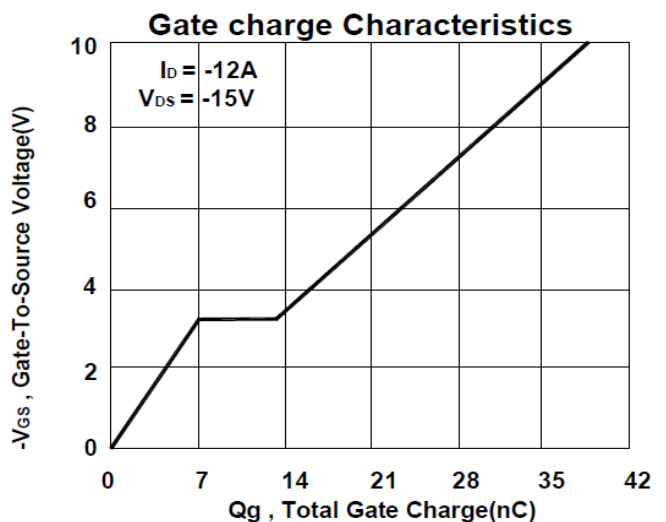
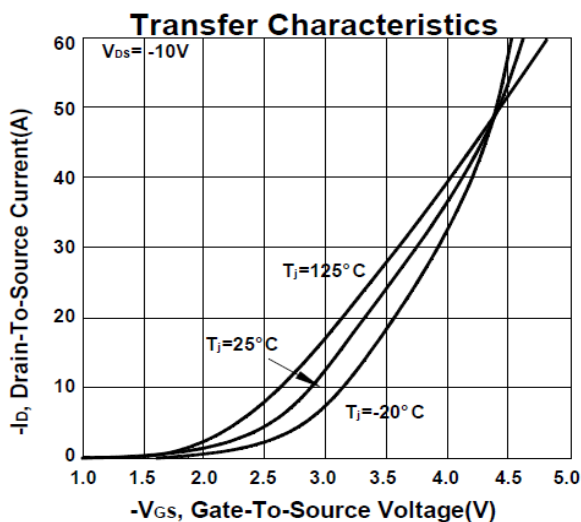
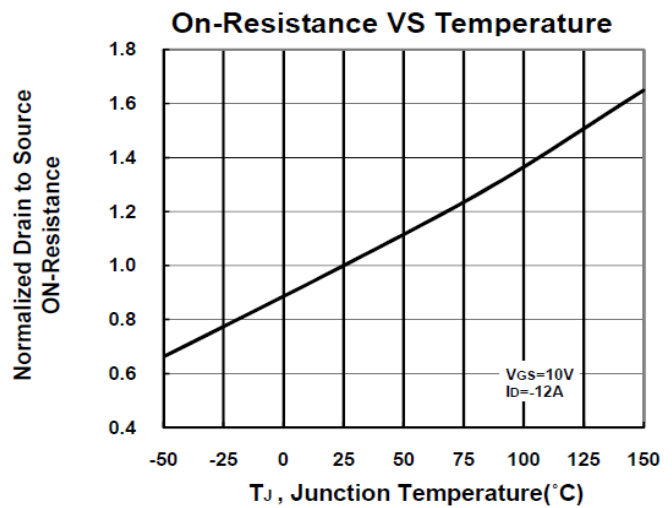
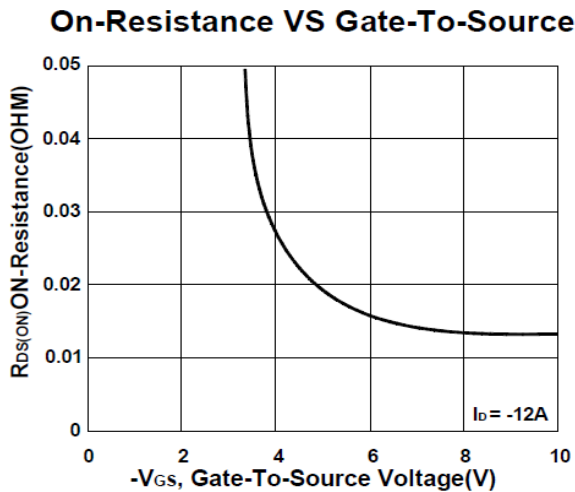
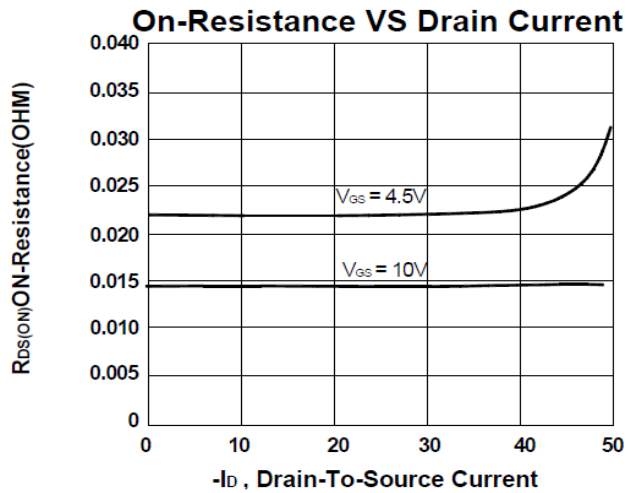
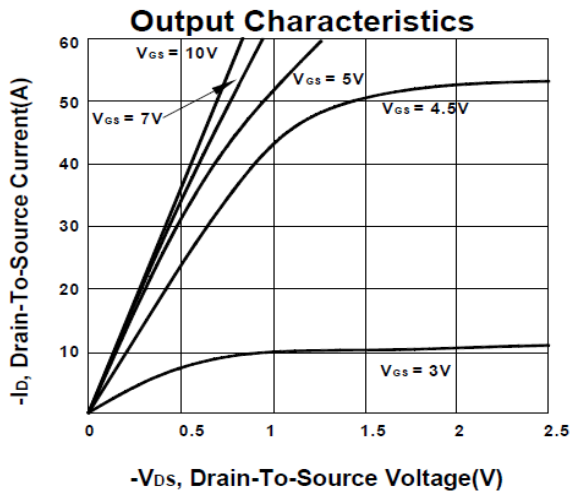
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Package limitation current is 30A.

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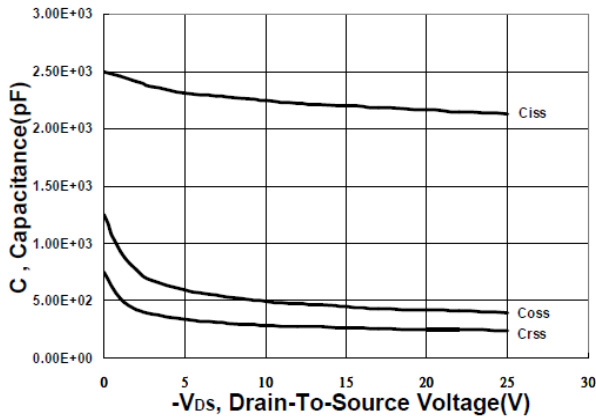
P-Channel Logic Level Enhancement Mode MOSFET



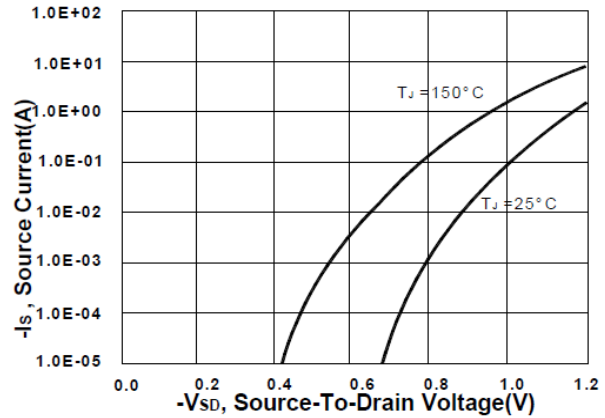
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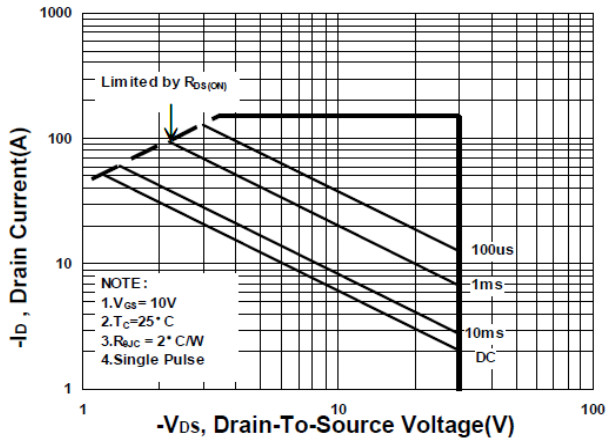
Capacitance Characteristic



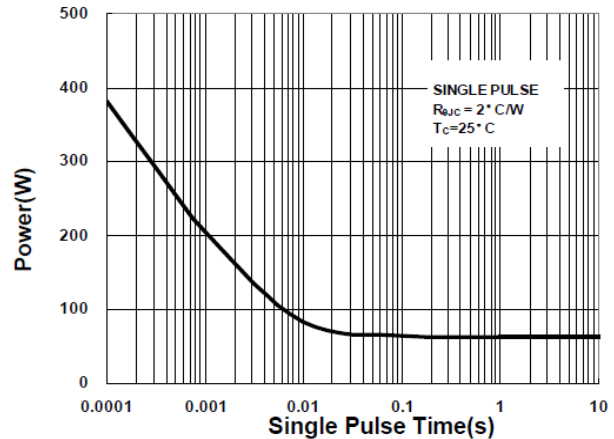
Body Diode Forward Voltage VS Source current



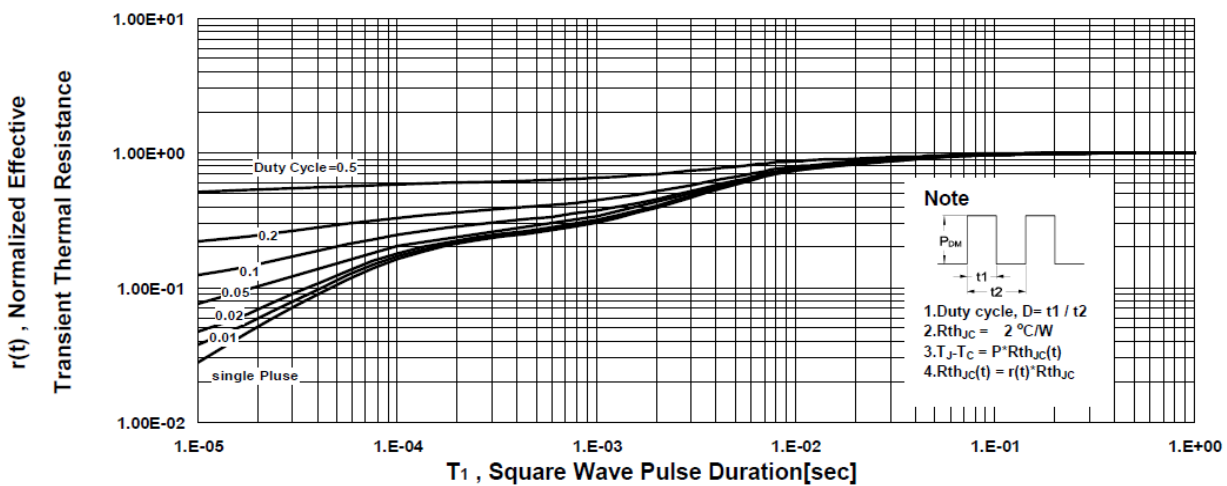
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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P-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

PDFN 5x6P MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8		5.15	J	3.33		3.78
B	5.44		5.9	K	0.9		
C	5.9		6.35	L	0.35		0.712
D	0.33		0.51	M	0°		12°
E		1.27		N	4.8		5.5
F	0.8		1.25	O	0.05		0.3
G	0.15		0.34	P	0.06		0.2
H	3.61		4.31	S	3.69		4.19
I	0.35		0.71				

