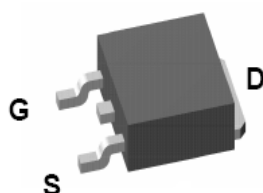


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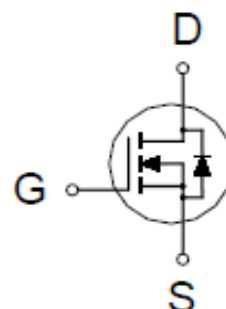
N-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
25V	90mΩ @ $V_{GS} = 10V$	12A



TO-252



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	12	A
	$T_C = 100\text{ }^{\circ}\text{C}$		8	
Pulsed Drain Current ¹		I_{DM}	45	
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	60	mJ
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	48	W
	$T_C = 100\text{ }^{\circ}\text{C}$		20	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^{\circ}\text{C}$
Lead Temperature ($^1/_{16}$ " from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		3	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		75	
Case-to-Heatsink	$R_{\theta CS}$	1		

¹Pulse width limited by maximum junction temperature.

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N-Channel Logic Level Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	25			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.8	1.2	2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$			25	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125^{\circ}C$			250	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	12			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 5V, I_D = 12A$		70	120	mΩ
		$V_{GS} = 10V, I_D = 12A$		50	90	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 15V, I_D = 12A$		16		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		450		pF
Output Capacitance	C_{oss}			200		
Reverse Transfer Capacitance	C_{rss}			60		
Total Gate Charge ²	Q_g	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = 10V, I_D = 6A$		15		nC
Gate-Source Charge ²	Q_{gs}			2.0		
Gate-Drain Charge ²	Q_{gd}			7.0		
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = 15V, R_L = 1\Omega, I_D \cong 12A, V_{GS} = 10V, R_{GS} = 2.5\Omega$		6.0		nS
Rise Time ²	t_r			6.0		
Turn-Off Delay Time ²	$t_{d(off)}$			20		
Fall Time ²	t_f			5.0		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I_S				12	A
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.5	V
Reverse Recovery Time	t_{rr}			30		nS
Reverse Recovery Charge	Q_{rr}			0.043		μC

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

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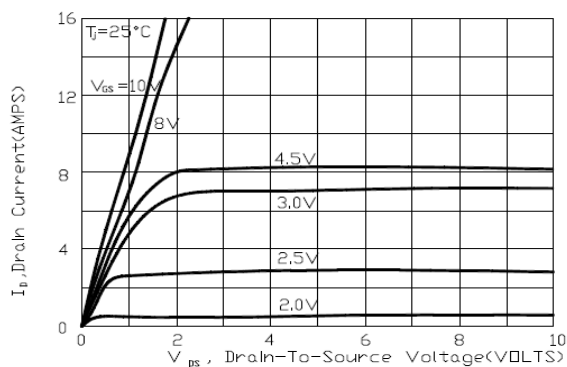


Fig.1 On-Resistance Variation with Temperature

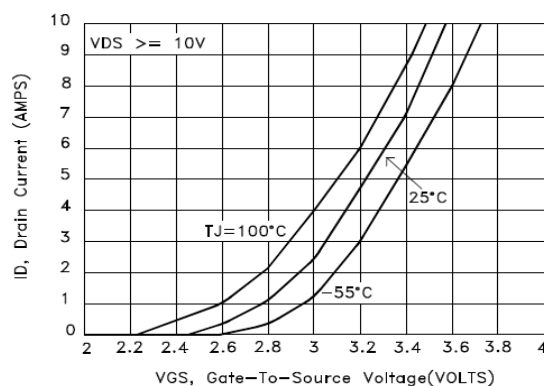


Fig.2 Transfer Characteristics

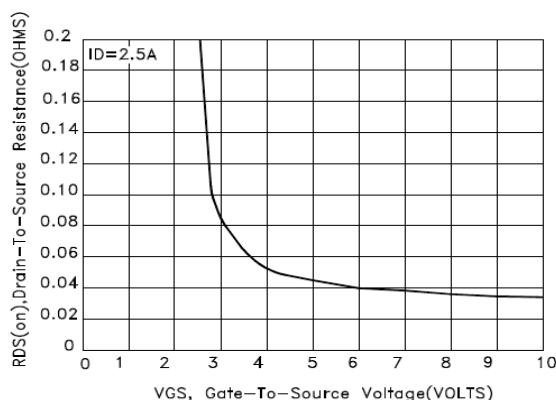


Fig.3 On-Resistance versus Gate-To-Source Voltage

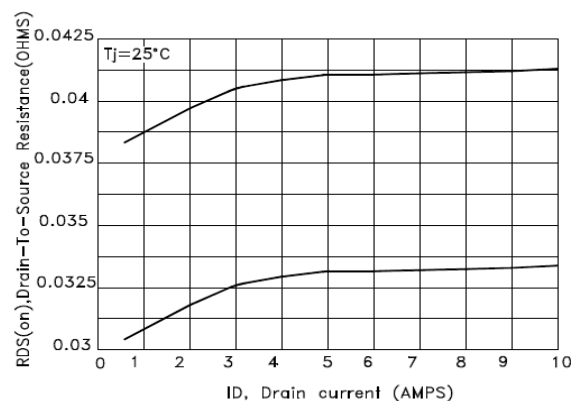


Fig.4 On-Resistance versus Drain Current and Gate Voltage

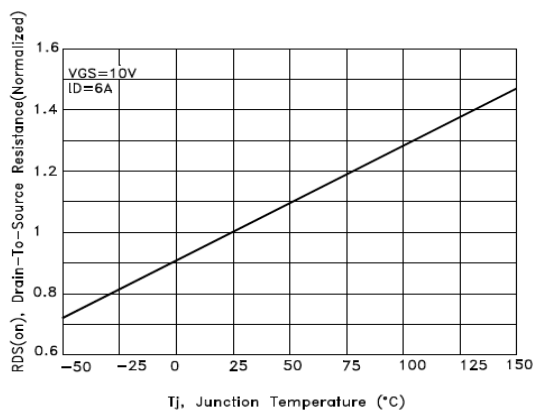


Fig.5 On-Resistance Variation with Temperature

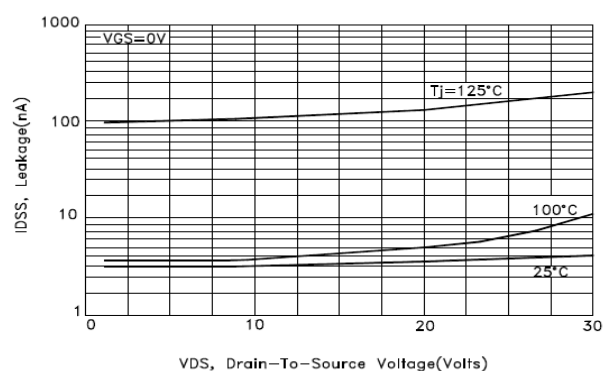


Fig.6 Drain-To-Source Leakage Current versus Voltage

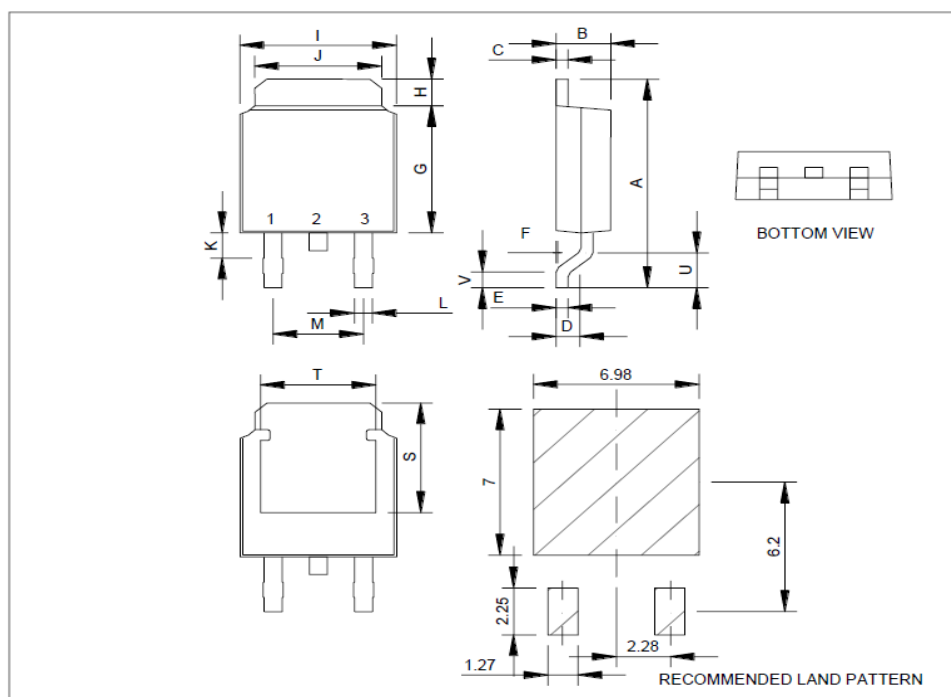
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N-Channel Logic Level Enhancement Mode MOSFET

Package Dimension

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	8.9	10	10.41	J	4.8		5.64
B	2.1	2.2	2.4	K	0.15		1.1
C	0.4	0.5	0.61	L	0.4	0.76	0.89
D	0.82	1.2	1.5	M	4.2	4.58	5
E	0.4	0.5	0.61	S	4.9	5.1	5.3
F	0		0.2	T	4.6	4.75	5.44
G	5.3	6.1	6.3	U	1.4		1.78
H	0.9		1.7	V	0.55	1.25	1.7
I	6.3	6.5	6.8				



*因为各家封装模具不同而外观略有所差异，不影响电性及Layout。