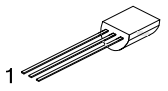
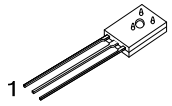
# MJE13002

**NPN EPITAXIAL SILICON TRANSISTOR**

## HIGH VOLTAGE FAST-SWITCHING NPN POWER TRANSISTOR




TO-92




TO-126

### ■ DESCRIPTION

The UTC **MJE13002** designed for use in high–volatge, high speed,power switching in inductive circuit, It is particularly suited for 115 and 220V switchmode applications such as switching regulator's,inverters, DC-DC converter, Motor control, Solenoid/Relay drivers and deflection circuits.

### ■ FEATURES

*Collector-Emitter Sustaining Voltage:
$V_{CEO}$ (sus)=300V.
*Collector-Emitter Saturation Voltage:
$V_{CE(sat)}$=1.0V(Max.) @Ic=1.0A, IB =0.25A
*Switch Time- tf =0.7μs(Max.) @Ic=1.0A.

### ■ ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | Packing |
|---|---|---|---|---|---|---|
| Lead Free | Halogen Free | | 1 | 2 | 3 | |
| MJE13002L-x-T92-B | MJE13002G-x-T92-B | TO-92 | B | C | E | Tape Box |
| MJE13002L-x-T92-K | MJE13002G-x-T92-K | TO-92 | B | C | E | Bulk |
| MJE13002L-x-T92-R | MJE13002G-x-T92-R | TO-92 | B | C | E | Tape Reel |
| MJE13002L-x-T60-T | MJE13002G-x-T60-T | TO-126 | B | C | E | Tube |

MJE13002L-x-T92-K
(1) Packing Type
(2) Package Type
(3) Rank
(4) Lead Free

(1) B: Tape Box, K: Bulk, R: Tape Reel, T: Tube
(2) T92: TO-92, T60: TO-126
(3) x: refer to Classification of $h_{FE1}$
(4) G: Halogen Free, L: Lead Free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## ■ ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Collector-Emitter Voltage | | $V_{CEO(SUS)}$ | 300 | V |
| Collector-Emitter Voltage | | $V_{CEV}$ | 600 | V |
| Emitter Base Voltage | | $V_{EBO}$ | 9 | V |
| Collector Current | Continuous | $I_C$ | 1.5 | A |
| | Peak (1) | $I_{CM}$ | 3 | |
| Base Current | Continuous | $I_B$ | 0.75 | A |
| | Peak (1) | $I_{BM}$ | 1.5 | |
| Emitter Current | Continuous | $I_E$ | 2.25 | A |
| | Peak (1) | $I_{EM}$ | 4.5 | |
| Total Power Dissipation | TA=25°C | $P_D$ | 1.4 | Watts |
| | Derate above 25°C | | 11.2 | MW/°C |
| | TC=25°C | | 40 | Watts |
| | Derate above 25°C | | 320 | MW/°C |
| Junction Temperature | | $T_J$ | 150 | °C |
| Storage Temperature | | $T_{STG}$ | -65 to +150 | °C |

## ■ THERMAL CHARACTERISTICS

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Junction to Case | TO-92 | $\theta_{JC}$ | 25 | °C/W |
| | TO-126 | | 3.12 | |
| Junction to Ambient | TO-92 | $\theta_{JA}$ | 122 | °C/W |
| | TO-126 | | 89 | |
| Maximum Load Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds | | $T_L$ | 275 | °C |

Note: 1. Pulse Test : Pulse Width=5ms,Duty Cycle≤10%

2. Designer 's Data for "Worst Case" Conditions – The Designer 's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves – representing boundaries on device characteristics – are given to facilitate "Worst case" design.

## ■ ELECTRICAL CHARACTERISTICS ($T_C$=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS (1)** | | | | | | |
| Collector-Emitter Sustaining Voltage | $V_{CEO(SUS)}$ | $I_C$=10 mA , $I_B$=0 | 300 | | | |
| Collector Cutoff Current | $I_{CEV}$ | $V_{CEV}$=Rated Value, $V_{BE}$(off)=1.5 V | | | 1 | |
| | | $V_{CEV}$=Rated Value, $V_{BE}$(off)=1.5V,Tc=100°C | | | 5 | |
| **SECOND BREAKDOWN** | | | | | | |
| Second Breakdown Collector Current with bass forward biased (See Figure 5) | $I_S/I_B$ | | | | | |
| Clamped Inductive SOA with base reverse biased (See Figure 6) | $R_{BSOA}$ | | | | | |
| DC Current Gain | $h_{FE1}$ | $I_C$=0.5 A, $V_{CE}$=2 V | 8 | | 40 | |
| | $h_{FE2}$ | $I_C$=1 A, $V_{CE}$=2 V | 5 | | 25 | |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)}$ | $I_C$=0.5A, $I_B$=0.1A | | | 0.5 | V |
| | | $I_C$=1A, $I_B$=0.25A | | | 1 | |
| | | $I_C$=1.5A, $I_B$=0.5A | | | 3 | |
| | | $I_C$=1A, $I_B$=0.25A,$T_C$=100°C | | | 1 | |
| Base-Emitter Saturation Voltage | $V_{BE(SAT)}$ | $I_C$=0.5A, $I_B$=0.1A | | | 1 | V |
| | | $I_C$=1A, $I_B$=0.25 A | | | 1.2 | |
| | | $I_C$=1A, $I_B$=0.25A,$T_C$=100°C | | | 1.1 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Current-Gain-Bandwidth Product | $f_T$ | $I_C$=100mA, $V_{CE}$=10 V, f=1MHz | 4 | 10 | | MHz |
| Output Capacitance | Cob | $V_{CB}$=10V, $I_E$=0, f=0.1MHz | | 21 | | pF |
| **SWITCHING CHARACTERISTICS (TABLE 1)** | | | | | | |
| Delay Time | $t_d$ | $V_{CC}$=125V, $I_C$=1A, $I_{B1}$=$I_{B2}$=0.2A, $t_P$=25μs, Duty Cycle≤1% | | 0.05 | 0.1 | μs |
| Rise Time | $t_r$ | | | 0.5 | 1 | μs |
| Storage Time | $t_s$ | | | 2 | 4 | μs |
| Fall Time | $t_f$ | | | 0.4 | 0.7 | μs |
| **INDUCTIVE LOAD, CLAMPED (TABLE 1, FIGURE 7)** | | | | | | |
| Storage Time | $t_{sv}$ | $I_C$=1A,Vclamp=300V, $I_{B1}$=0.2A,$V_{BE}$(off)=5V,$T_C$=100°C | | 1.7 | 4 | μs |
| Crossover Time | $t_c$ | | | 0.29 | 0.75 | μs |
| Fall Time | $t_{fi}$ | | | 0.15 | | μs |

## ■ CLASSIFICATION OF $h_{FE1}$

| RANK | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| RANGE | 8 ~ 16 | 15 ~ 21 | 20 ~ 26 | 25 ~ 31 | 30 ~ 36 | 35 ~ 40 |

## ■ APPLICATION INFORMATION

Table 1.Test Conditions for Dynamic Performance

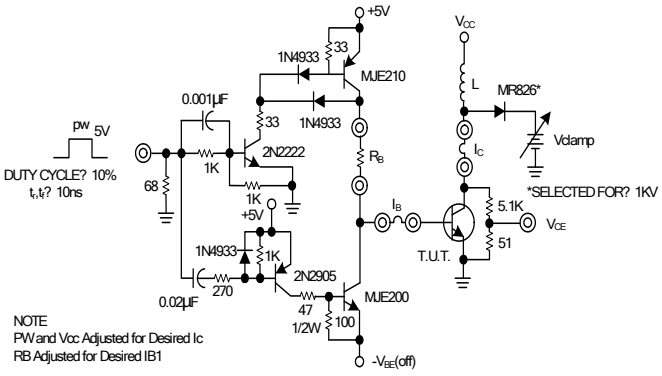
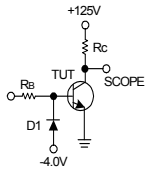
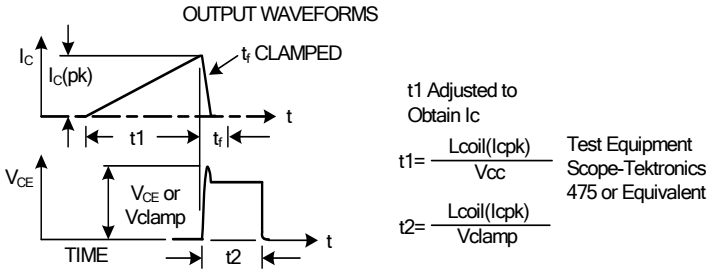
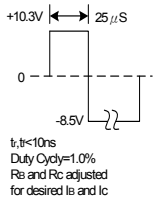
| | Reverse Bias Safe Operating Area and Inductive Switching | Resistive Switching |
|---|---|---|
| Test Circuits |  |  |
| Circuit Values | Coil Data :<br>VCC=20V<br>Ferroxcube core #6656<br>Vclamp=300V<br>Full Bobbin ( ~ 200 Turns) #20<br>GAP for 30 mH/2 A<br>Lcoil=50mH | VCC=125V<br>RC=125Ω<br>D1=1N5820 or Equiv.<br>RB=47Ω |
| Test Waveforms | Output Waveforms<br>  |  |

Table 2. Typical Inductive Switching Performance

| $I_C$ (AMP) | $T_C$ (°C) | $T_{SV}$ (μs) | $T_{RV}$ (μs) | $T_{FI}$ (μs) | $T_{TI}$ (μs) | $T_C$ (μs) |
|---|---|---|---|---|---|---|
| 0.5 | 25<br>100 | 1.3<br>1.6 | 0.23<br>0.26 | 0.30<br>0.30 | 0.35<br>0.40 | 0.30<br>0.36 |
| 1 | 25<br>100 | 1.5<br>1.7 | 0.10<br>0.13 | 0.14<br>0.26 | 0.05<br>0.06 | 0.16<br>0.29 |
| 1.5 | 25<br>100 | 1.8<br>3 | 0.07<br>0.08 | 0.10<br>0.22 | 0.05<br>0.08 | 0.16<br>0.28 |

Note: All Data Recorded in the inductive Switching Circuit Table 1

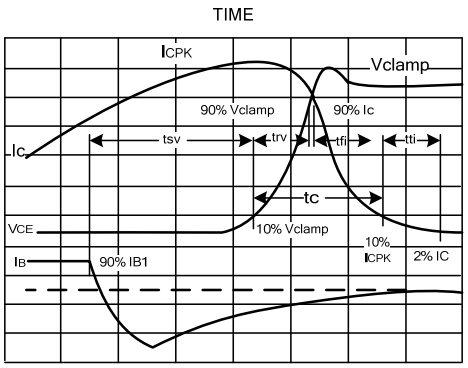



Fig 1. Inductive Switching Measurements

## ■ SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase, However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each wave form to determine the total switching time, For this reason, the following new terms have been defined.

$t_{SV}$=Voltage Storage Time, 90% IB1 to 10% Vclamp

$t_{RV}$=Voltage Rise Time, 10-90% Vclamp

$t_{FI}$=Current Fall Time, 90-10% $I_C$

$t_{TI}$=Current Tail, 10-2% $I_C$

$t_C$=Crossover Time, 10% Vclamp to 10% $I_C$

An enlarged portion of the inductive switching waveforms is shown in Figure 1 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222:

PSWT=1/2 VccIc (tc)f

In general, trv + tfi ≒ tc. However, at lower test currents this relationship may not be valid.

As is common with most switching transistor, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (tc and tsv) which are guaranteed at 100°C.

**RESISTIVE SWITCHING PERFORMANCE**

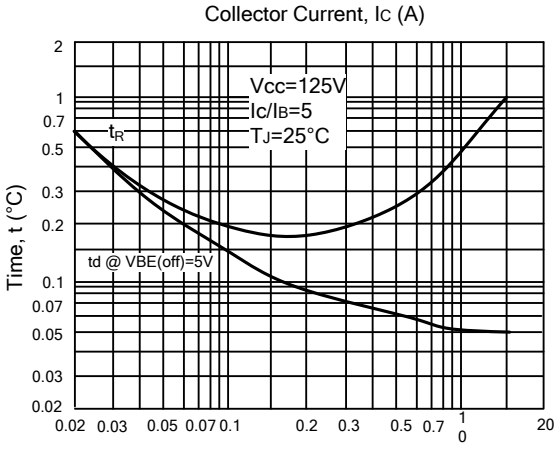



Fig 2. Turn-On Time

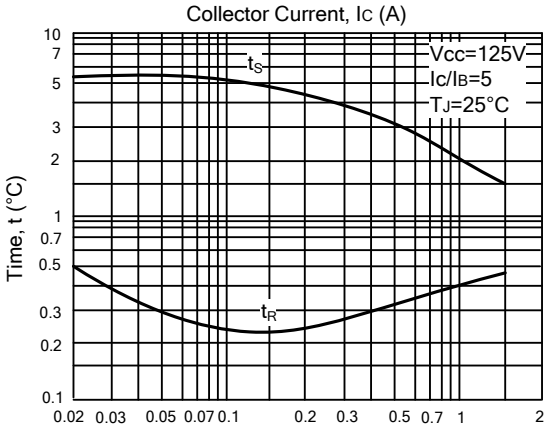



Fig 3. Turn-Off Time

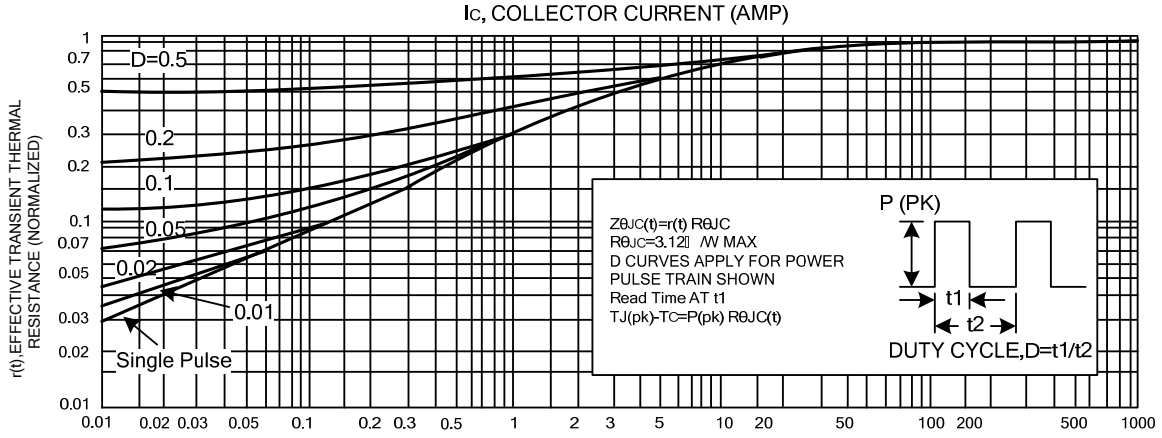



Fig 4. Thermal Response

## ■ SAFE OPERATING AREA INFORMATION

**FORWARD BIAS**

There are two limitations on the power handling ability of a transistor: average junction temperature and second break-down. Safe operating area curves indicate Ic – VCE limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on Tc=25°C; TJ(pk) is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when Tc≧25°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 5 may be found at any case tem-perature by using the appropriate curve on Figure 7.

$T_J$(pk) may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

**REVERSE BIAS**

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current conditions during re-verse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an ava-lanche mode. Figure 6 gives RBSOA characteristics.

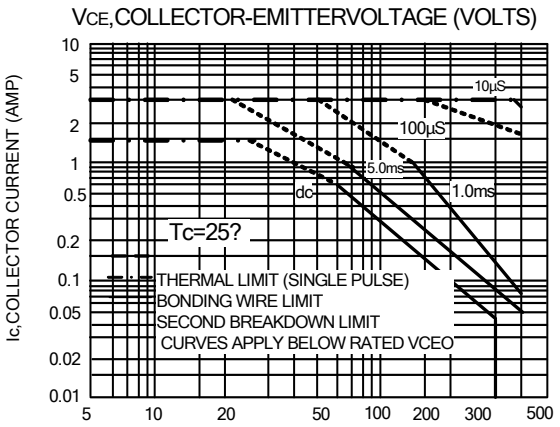



Fig 5. Active Region Safe Operating Area

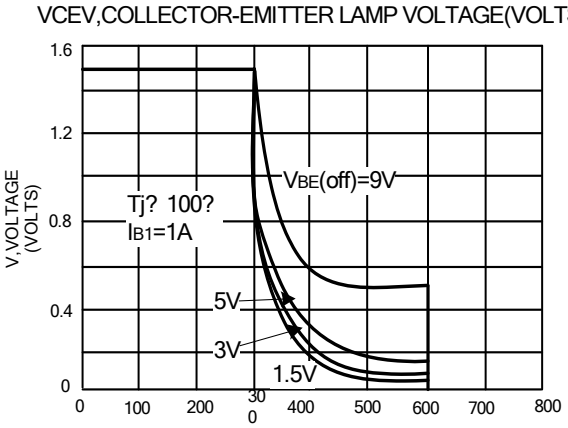



Fig 6. Reverse Bias Safe Operating Area

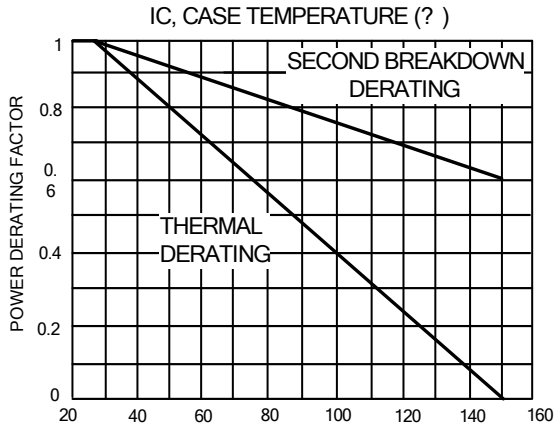
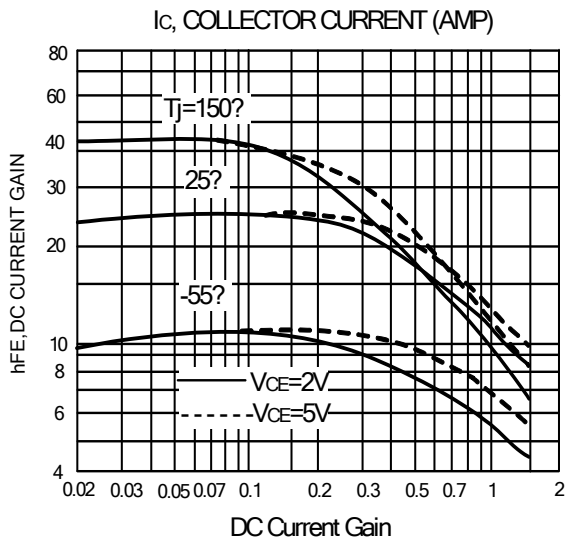
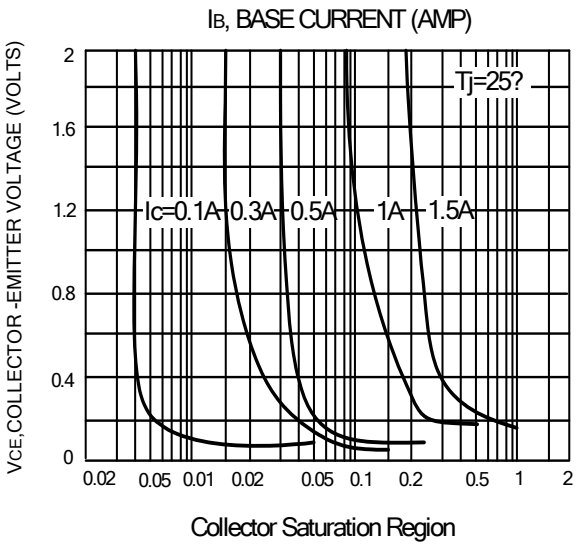
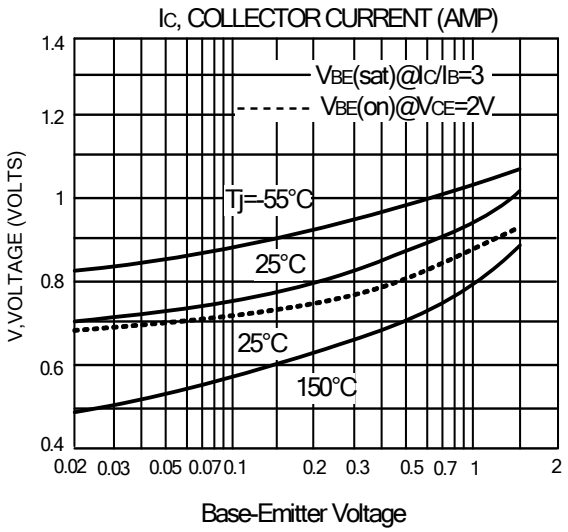


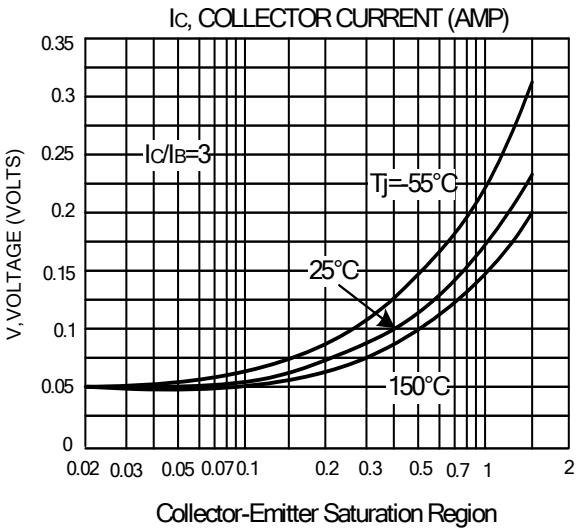

Fig 7. Forward Bias Power Derating

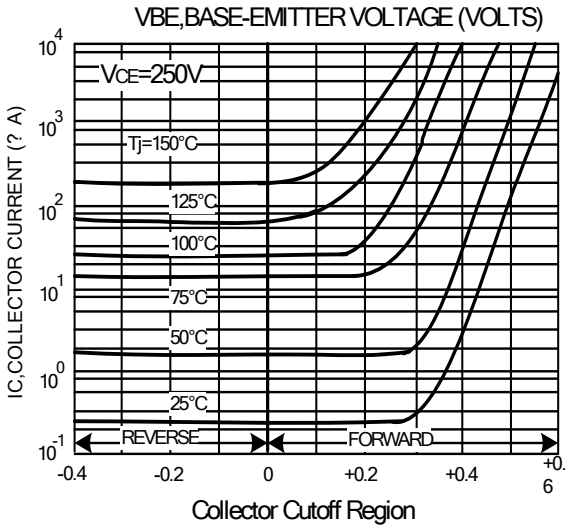
## ■ TYPICAL CHARACTERISTICS

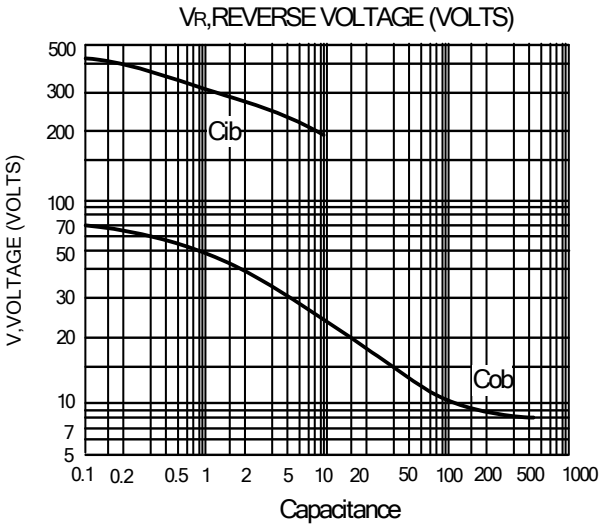


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