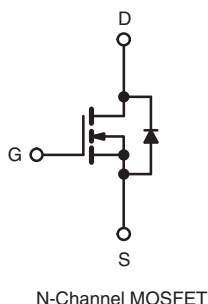
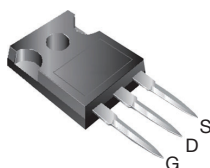


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.009
Q_g (Max.) (nC)	190	
Q_{gs} (nC)	55	
Q_{gd} (nC)	90	
Configuration	Single	

TO-247AC


FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Ultra Low On- Resistance
- Very Low Thermal Resistance
- Isolated Central Mounting Hole
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-247AC package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because its isolated mounting hole. It also provides greater creepage distances between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFP064PbF SiHFP064-E3
SnPb	IRFP064 SiHFP064

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	V_{GS} at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	A
		$T_C = 100\text{ }^{\circ}\text{C}$	
Pulsed Drain Current ^a	I_{DM}	520	
Linear Derating Factor		2.0	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	1000	mJ
Repetitive Avalanche Current ^a	I_{AR}	70	A
Repetitive Avalanche Energy ^a	E_{AR}	30	mJ
Maximum Power Dissipation	P_D	300	W
Peak Diode Recovery dV/dt ^c	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature) ^d	for 10 s	300	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes



- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 69\text{ }\mu\text{H}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 130\text{ A}$ (see fig. 12).
- $I_{SD} \leq 130\text{ A}$, $dI/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.
- Current limited by the package (die current = 130 A).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

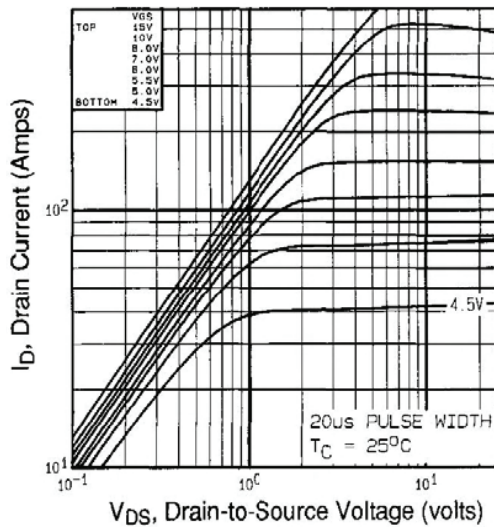
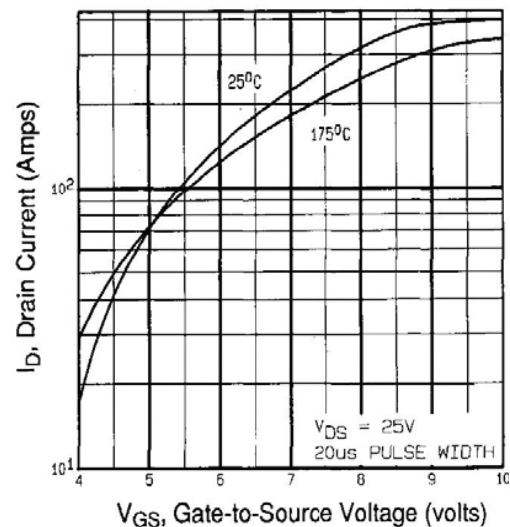
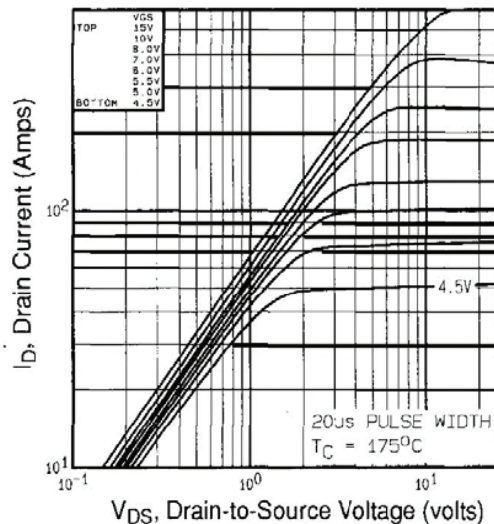
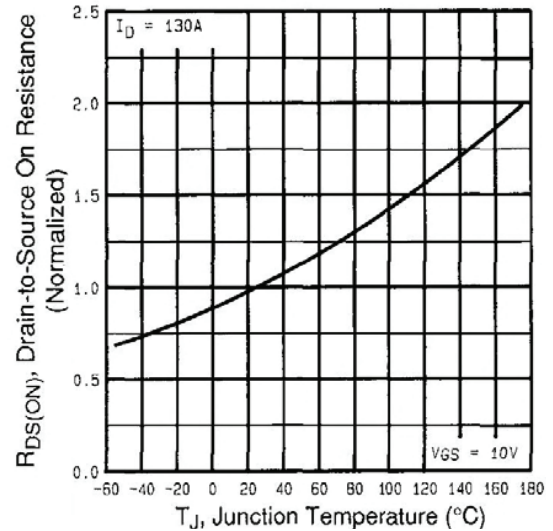
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.50	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.048	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 78 A ^b	-	-	0.009	Ω
Forward Transconductance	g _{fs}	V _{DS} = 25 V, I _D = 78 A ^b		38	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	7400	-	pF
Output Capacitance	C _{oss}			-	3200	-	
Reverse Transfer Capacitance	C _{rss}			-	540	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 130 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	190	nC
Gate-Source Charge	Q _{gs}			-	-	55	
Gate-Drain Charge	Q _{gd}			-	-	90	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 130 A, R _g = 4.3 Ω, R _D = 0.22 Ω, see fig. 10 ^b		-	21	-	ns
Rise Time	t _r			-	190	-	
Turn-Off Delay Time	t _{d(off)}			-	110	-	
Fall Time	t _f			-	190	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	5.0	-	nH
Internal Source Inductance	L _S			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	70 ^c	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	520	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 130 A, V _{GS} = 0 V ^b		-	-	3.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 130 A, dI/dt = 100 A/μs ^b		-	160	250	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.9	1.7	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- Current limited by the package (die current = 130 A).

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

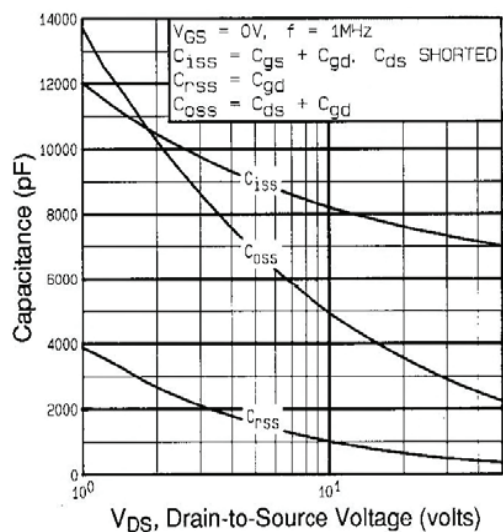


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

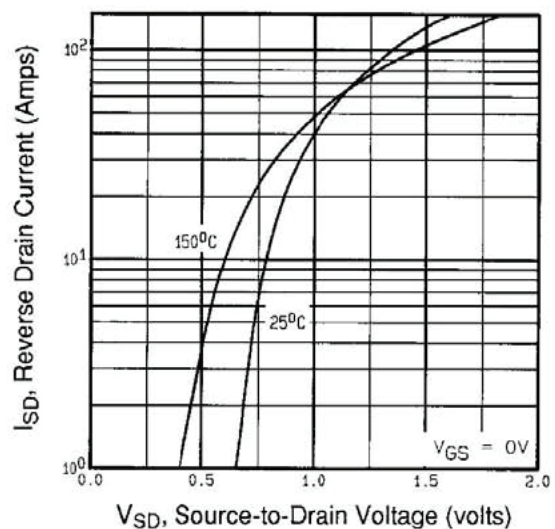


Fig. 7 - Typical Source-Drain Diode Forward Voltage

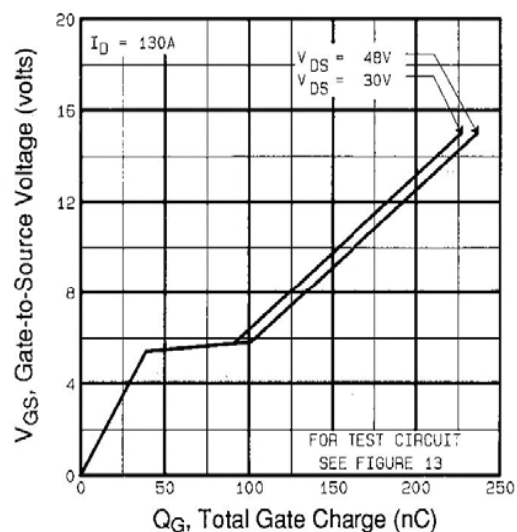


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

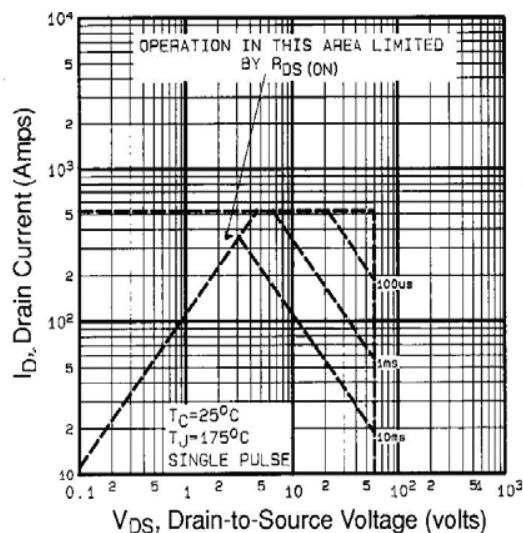


Fig. 8 - Maximum Safe Operating Area

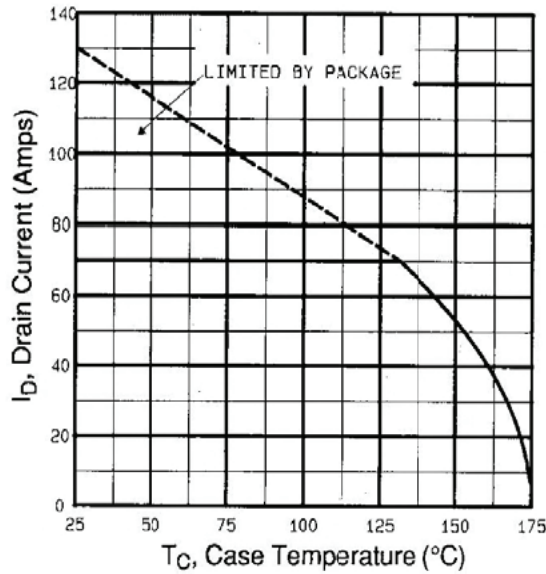


Fig. 9 - Maximum Drain Current vs. Case Temperature

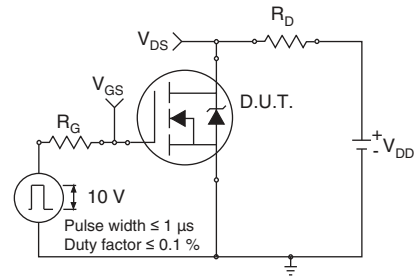


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

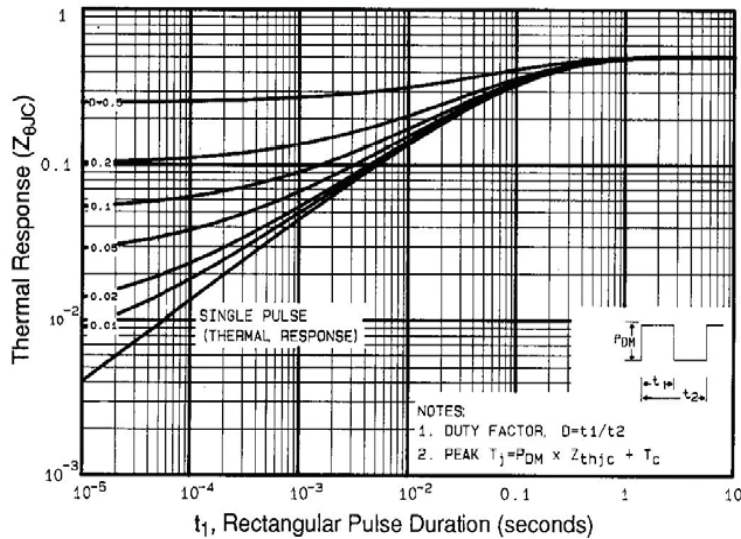


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

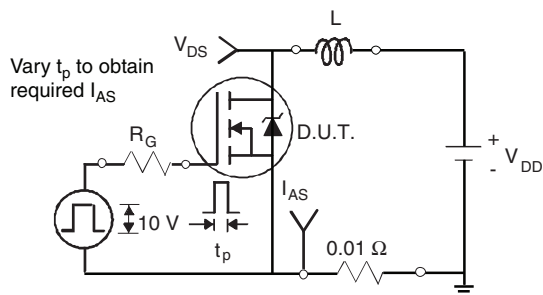


Fig. 12a - Unclamped Inductive Test Circuit

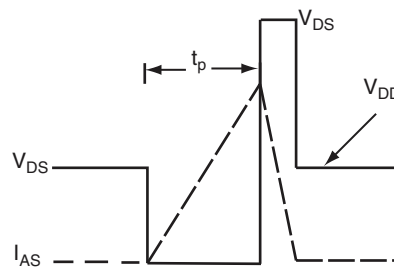


Fig. 12b - Unclamped Inductive Waveforms

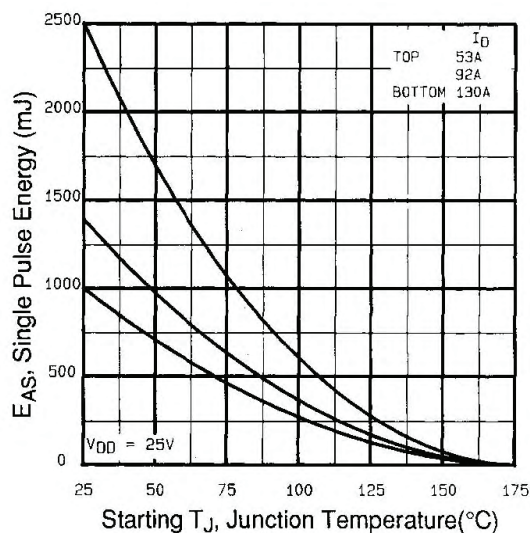


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

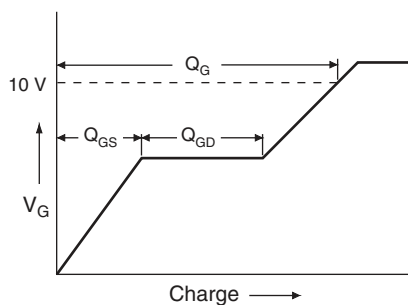


Fig. 13a - Basic Gate Charge Waveform

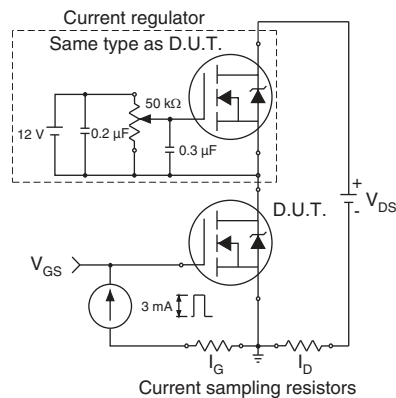
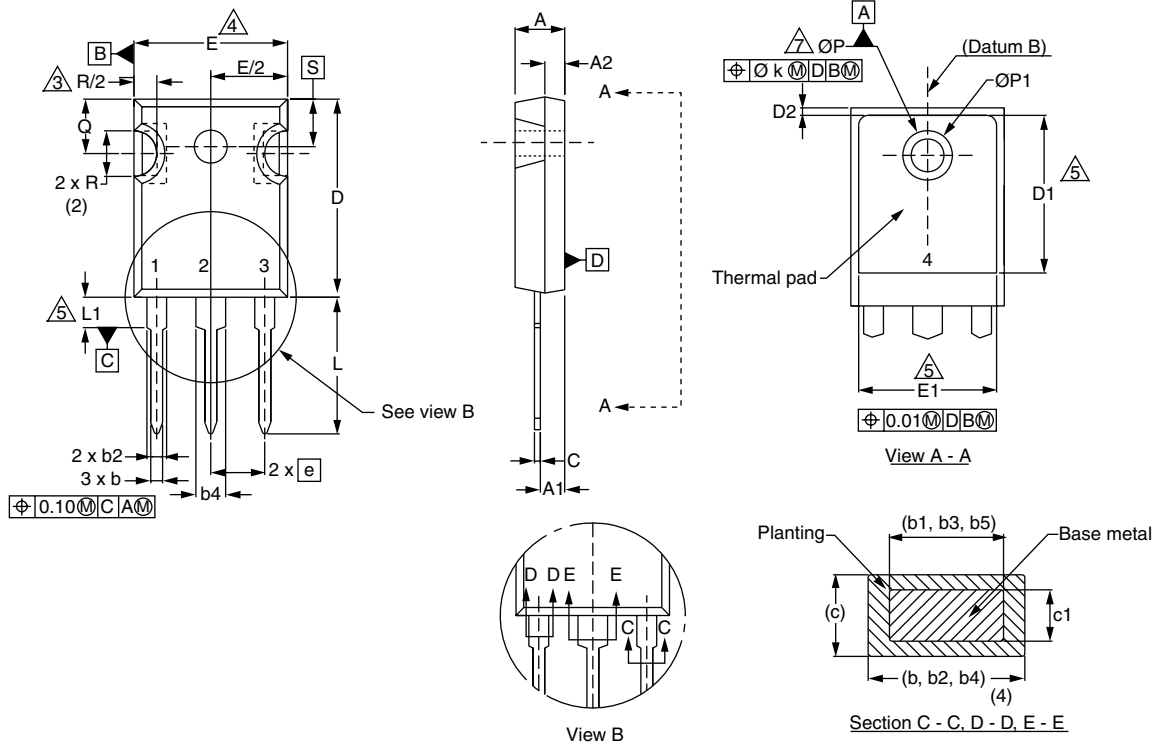


Fig. 13b - Gate Charge Test Circuit

a. $V_{GS} = 5 \text{ V}$ for logic level devices

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TO-247AC (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.65	5.31	0.183	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.65	2.39	0.065	0.094
b3	1.65	2.37	0.065	0.093
b4	2.59	3.43	0.102	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.70	0.776	0.815
D1	13.08	-	0.515	-

ECN: S-81920-Rev. A, 15-Sep-08
DWG: 5971

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.10	0.559	0.634
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.56	3.66	0.140	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.



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