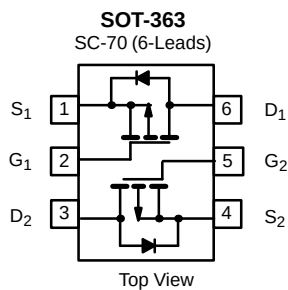




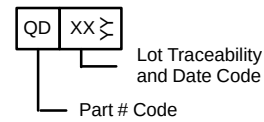
P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (mA)
-20	3.8 @ $V_{GS} = -4.5$ V	-180
	5.0 @ $V_{GS} = -2.5$ V	-100



Marking Code

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$ -180	mA
		$T_A = 70^\circ\text{C}$ -140	
Pulsed Drain Current	I_{DM}	-500	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$ 0.20	W
		$T_A = 70^\circ\text{C}$ 0.13	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	625	$^\circ\text{C/W}$

Notes

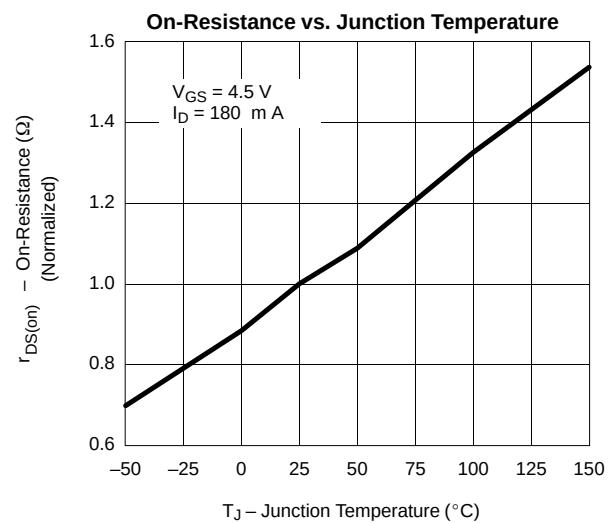
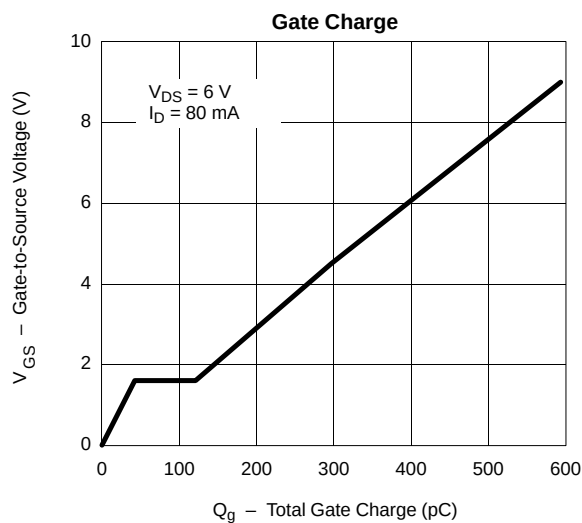
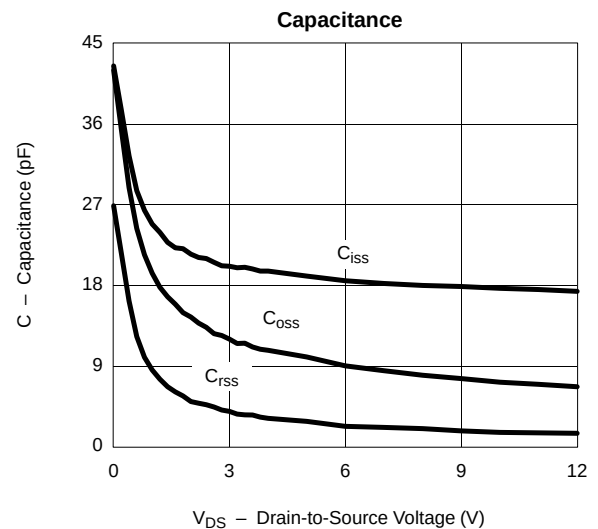
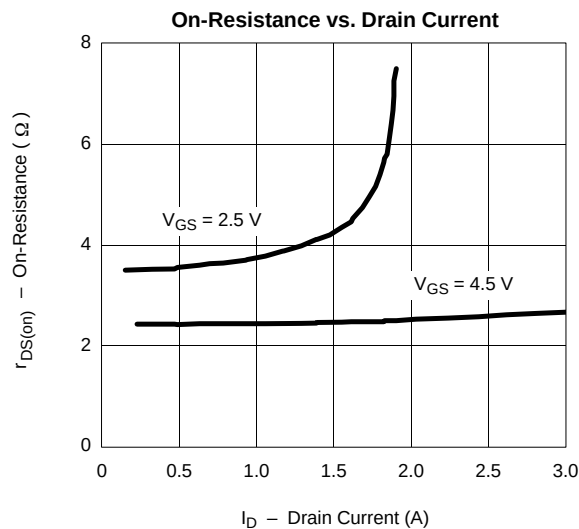
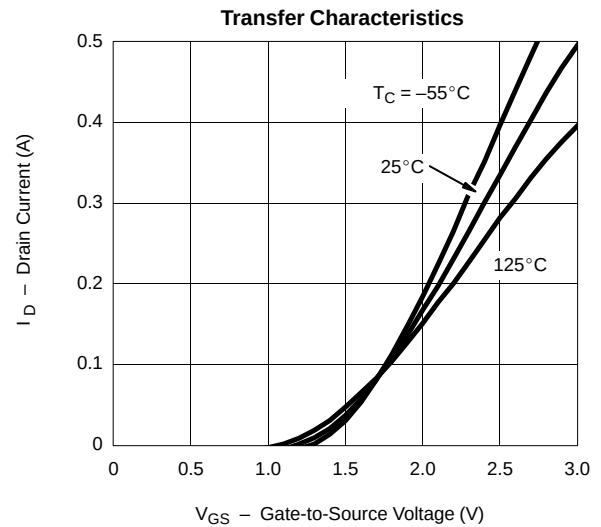
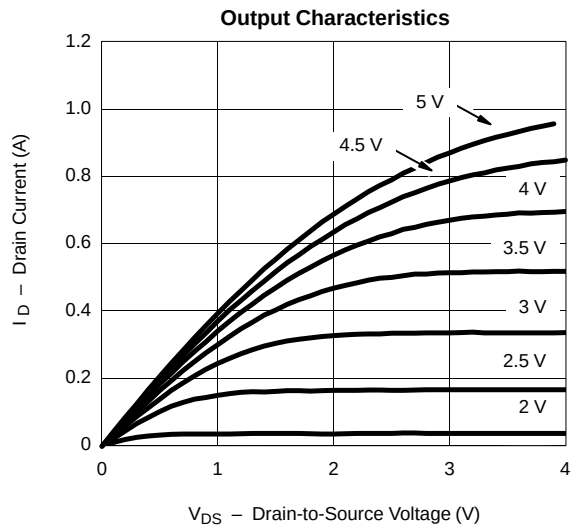
a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

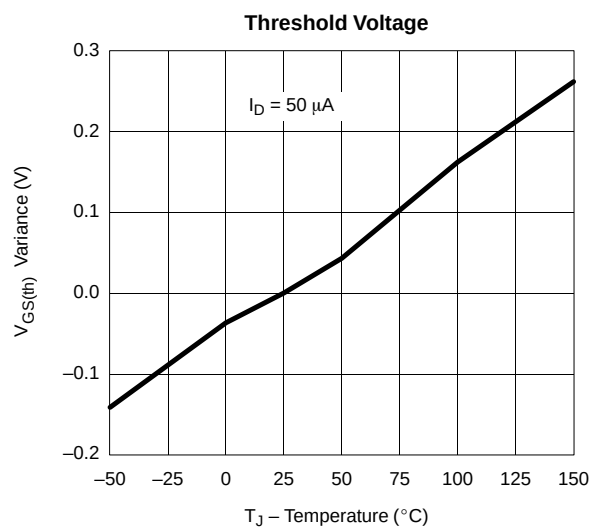
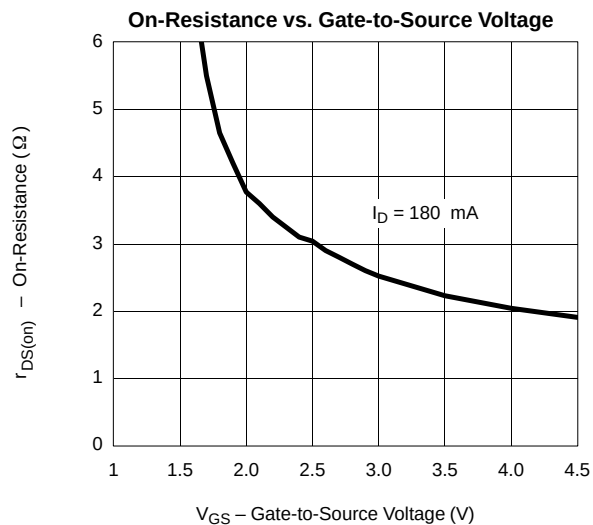
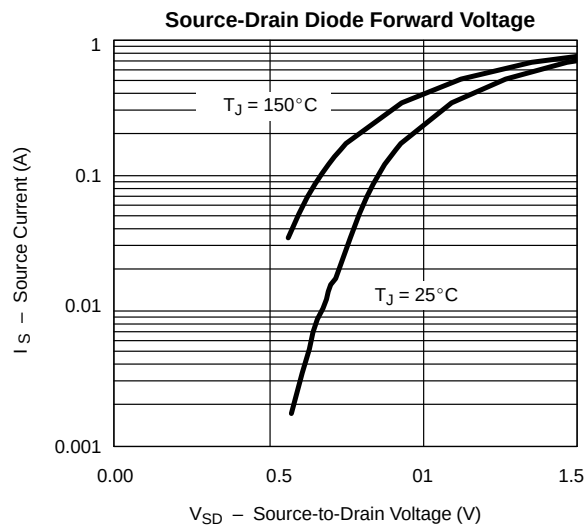


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = −10 μA	−20	−24		V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = −50 μA	−0.4	−0.9	−1.5	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V		±2	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = −20 V, V _{GS} = 0 V		−0.001	−100	
		V _{DS} = −20 V, V _{GS} = 0 V, T _J = 55°C			−1	μA
On-State Drain Current ^a	I _{D(on)}	V _{GS} ≤ −4.5 V, V _{DS} = −8.0 V	−400			mA
		V _{GS} ≤ −2.5 V, V _{DS} = −5.0 V	−120			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = −4.5 V, I _D = −180 mA		2.6	3.8	Ω
		V _{GS} = −2.5 V, I _D = −75 mA		4.0	5.0	
Forward Transconductance ^a	g _{fs}	V _{DS} = −2.5 V, I _D = −50 mA		200		mS
Diode Forward Voltage ^a	V _{SD}	I _S = −50 mA, V _{GS} = 0 V		−0.7	−1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} = −5.0 V, V _{GS} = −4.5 V, I _D = −100 mA		350	450	pC
Gate-Source Charge	Q _{gs}			25		
Gate-Drain Charge	Q _{gd}			125		
Input Capacitance	C _{iss}	V _{DS} = −5.0 V, V _{GS} = 0 V, f = 1 MHz		20		pF
Output Capacitance	C _{oss}			14		
Reverse Transfer Capacitance	C _{rss}			5		
Switching ^{b, c}						
Turn-On Delay Time	t _{d(on)}	V _{DD} = −3.0 V, R _L = 100 Ω I _D = −0.25 A, V _{GEN} = −4.5 V, R _G = 10 Ω		7	12	ns
Rise Time	t _r			25	35	
Turn-Off Delay Time	t _{d(off)}			19	30	
Fall Time	t _f			9	15	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. For design only, not subject to production testing.
c. Switching time is essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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