

N-Channel 40-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
40	0.0074 at $V_{GS} = 10$ V	70 ^a
	0.011 at $V_{GS} = 4.5$ V	67

FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- Low Threshold

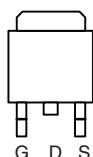


Available
RoHS*
COMPLIANT

APPLICATIONS

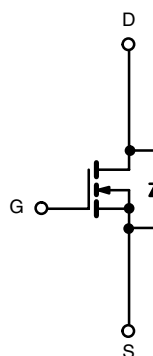
- Motor Control

TO-263



Top View

Ordering Information: SUM70N04-07L-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 125$ °C	
Pulsed Drain Current	I_{DM}	120	
Avalanche Current	I_{AR}	40	
Repetitive Avalanche Energy ^b	E_{AR}	80	mJ
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	W
		$T_A = 25$ °C ^d	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	40	°C/W
Junction-to-Case	R_{thJC}	1.4	

Notes:

a. Package limited.

b. Duty cycle ≤ 1 %.

c. See SOA curve for voltage derating.

d. When Mounted on 1" square PCB (FR-4 material).

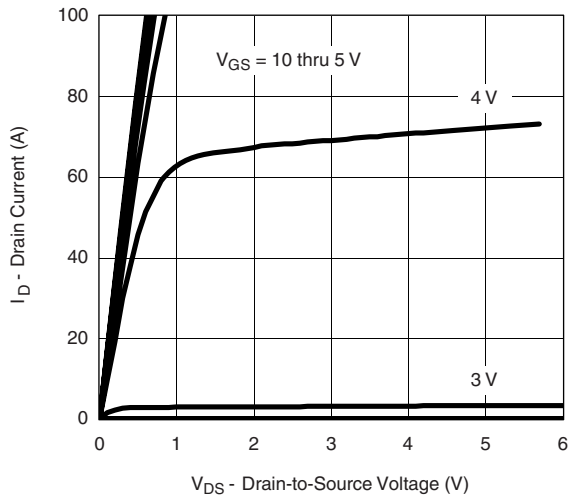
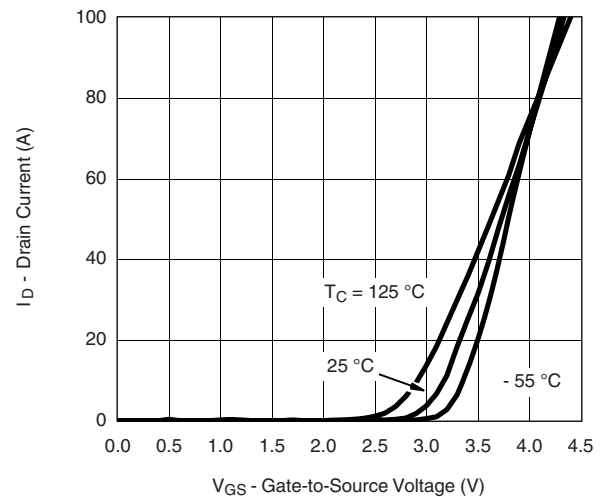
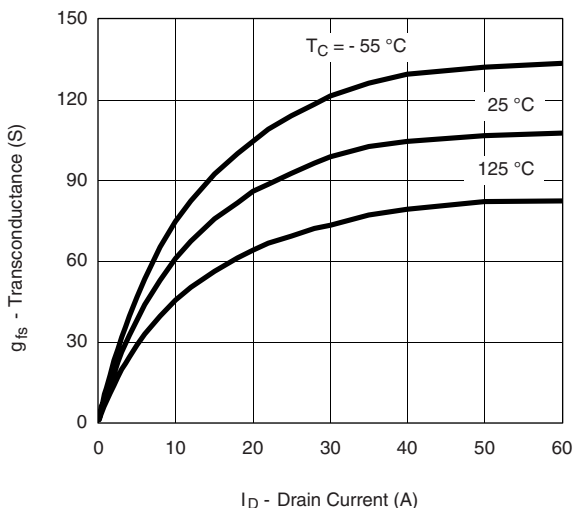
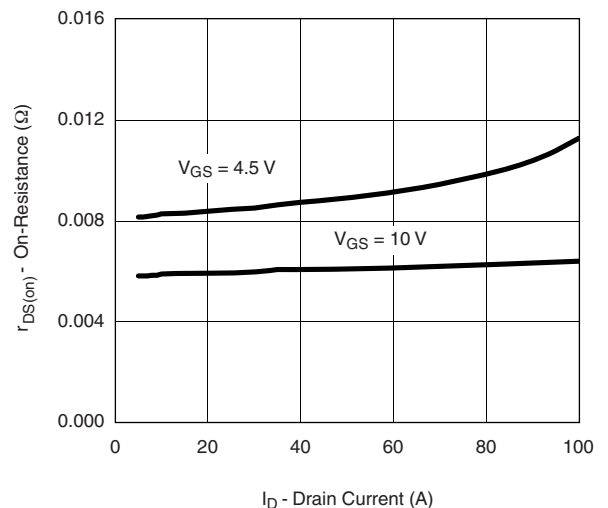
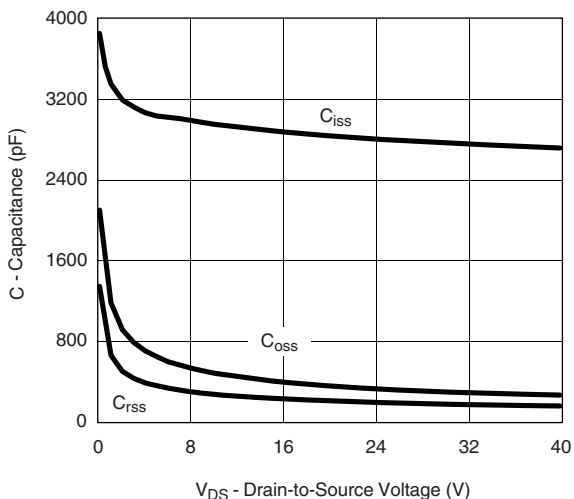
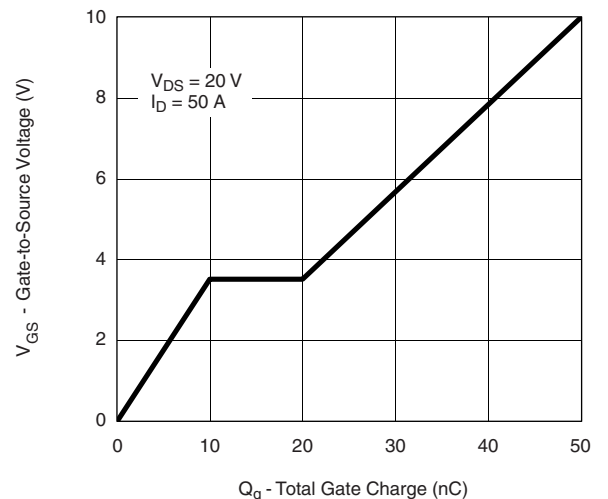
* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	40			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1		3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 32\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$			50	
		$V_{DS} = 32\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 175\text{ }^{\circ}\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	100			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$		0.006	0.0074	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$		0.0085	0.011	
		$V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$			0.012	
		$V_{GS} = 10\text{ V}$, $I_D = 30\text{ A}$, $T_J = 175\text{ }^{\circ}\text{C}$			0.015	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 30\text{ A}$	20			S
Dynamic ^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$		2800		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			190		
Total Gate Charge ^c	Q_g	$V_{DS} = 20\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 50\text{ A}$		50	75	nC
Gate-Source Charge ^c	Q_{gs}			10		
Gate-Drain Charge ^c	Q_{gd}			10		
Gate Resistance	R_G			2.0		Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 20\text{ V}$, $R_L = 0.4\text{ }\Omega$ $I_D \cong 50\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_G = 2.5\text{ }\Omega$		11	20	ns
Rise Time ^c	t_r			20	30	
Turn-Off Delay Time ^c	$t_{d(off)}$			40	60	
Fall Time ^c	t_f			15	25	
Source-Drain Diode Ratings and Characteristics $T_C = 25\text{ }^{\circ}\text{C}$ ^b						
Continuous Current	I_S				66	A
Pulsed Current	I_{SM}				100	
Forward Voltage ^a	V_{SD}	$I_F = 50\text{ A}$, $V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 50\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		30	50	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			1.6	2.4	A
Reverse Recovery Charge	Q_{rr}				0.024	0.06

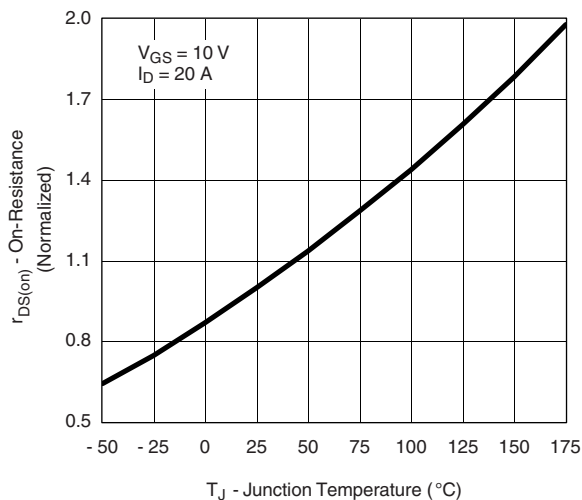
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

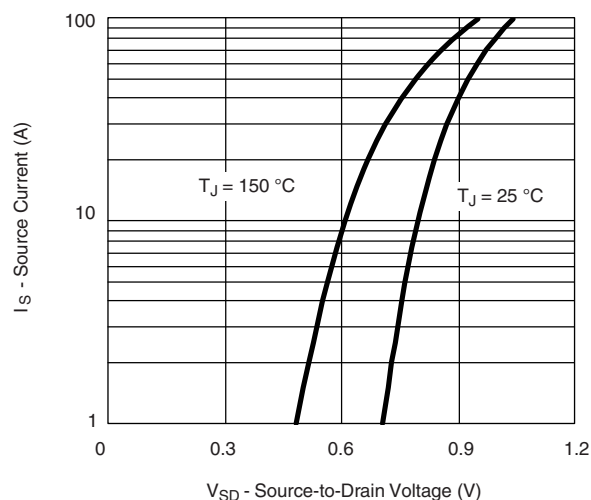
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

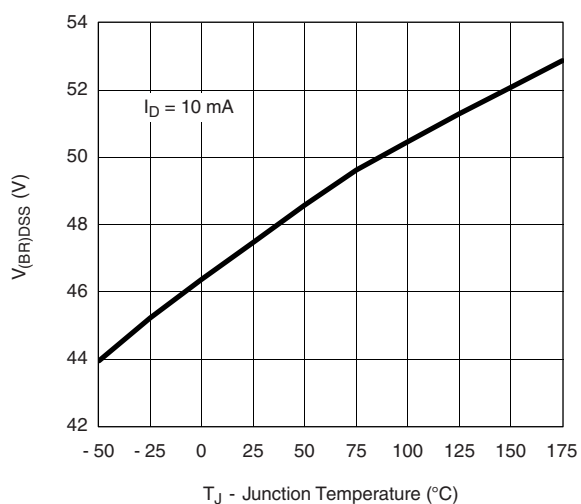
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



On-Resistance vs. Junction Temperature

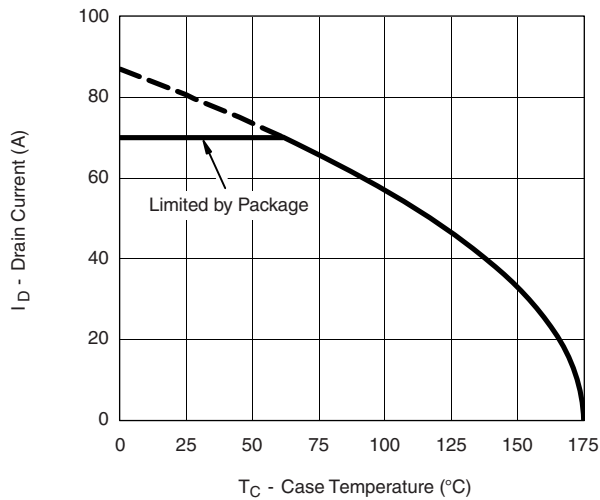


Source-Drain Diode Forward Voltage

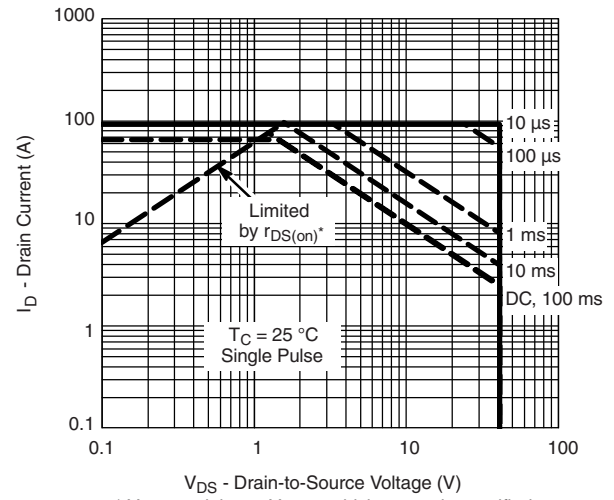


Drain Source Breakdown vs. Junction Temperature

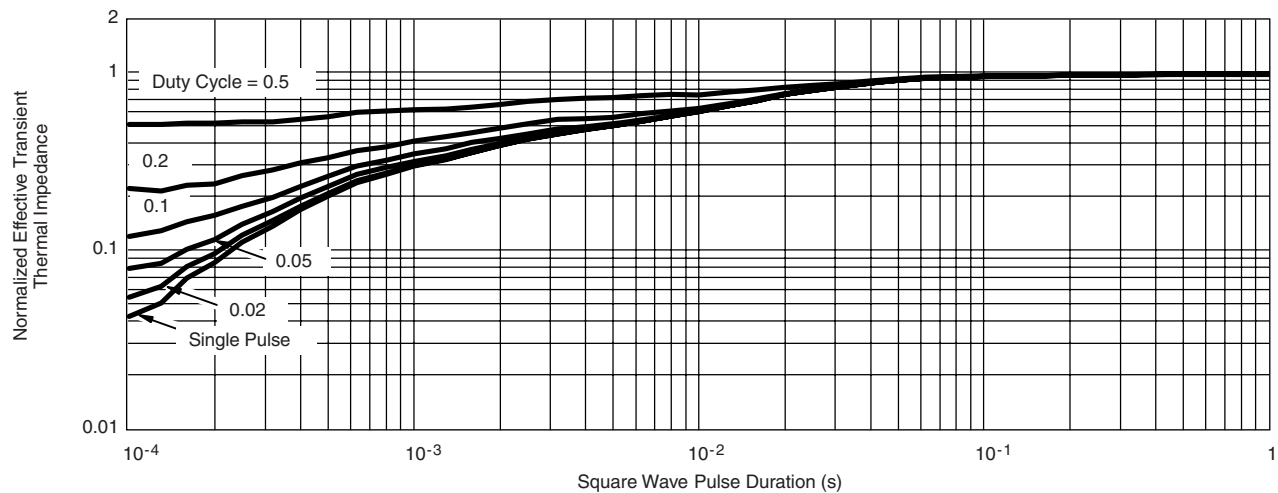
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



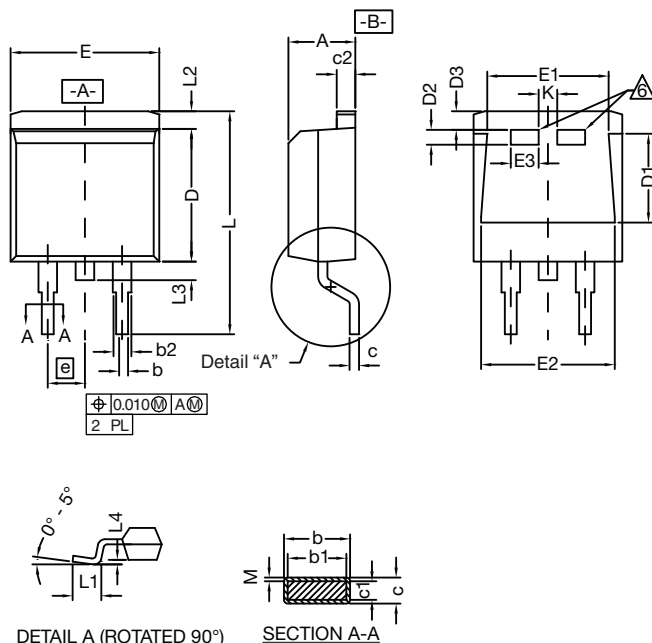
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72345>.

TO-263 (D²PAK): 3-LEAD

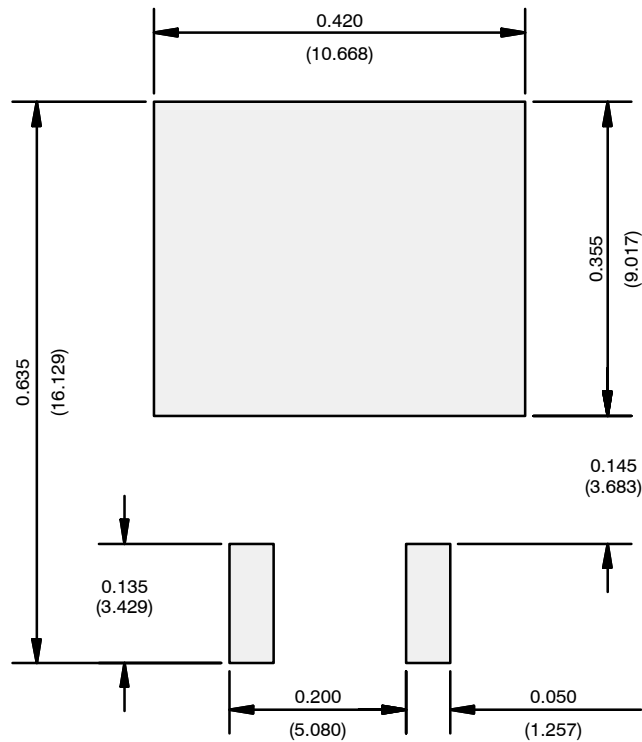


DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
[e]		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T10-0738-Rev. J, 03-Jan-11					
DWG: 5843					

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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